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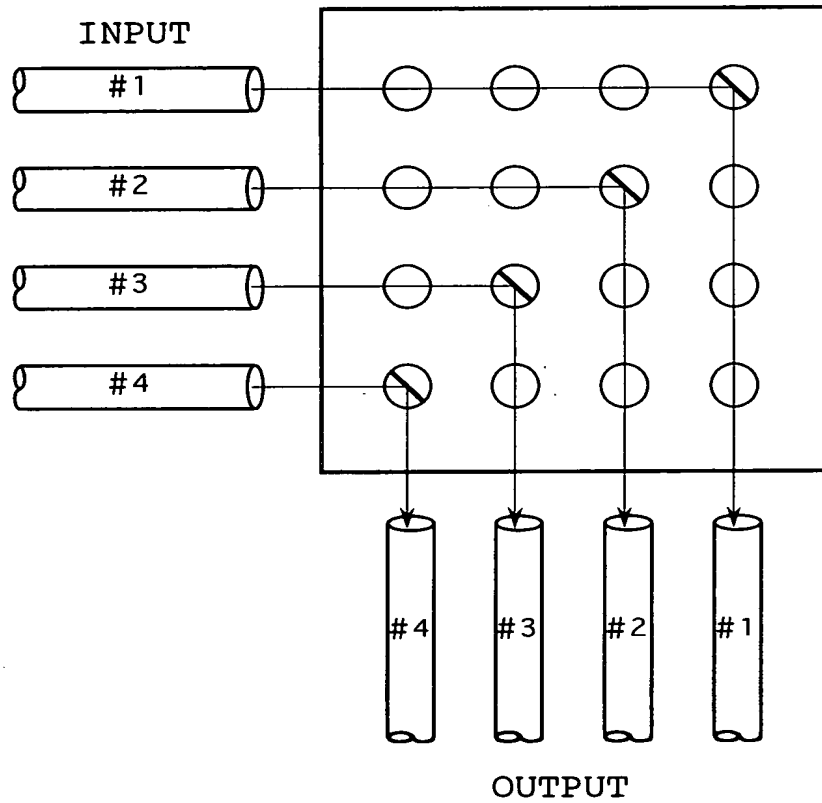
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FIG. 1

PRIOR ART



- ⊗ ; SWITCH CELL (ON STATE; MIRROR INSERTED)
- ; SWITCH CELL (OFF STATE; MIRROR NOT INSERTED)

09924506-000901

106080" 90912660

FIG.2

PRIOR ART

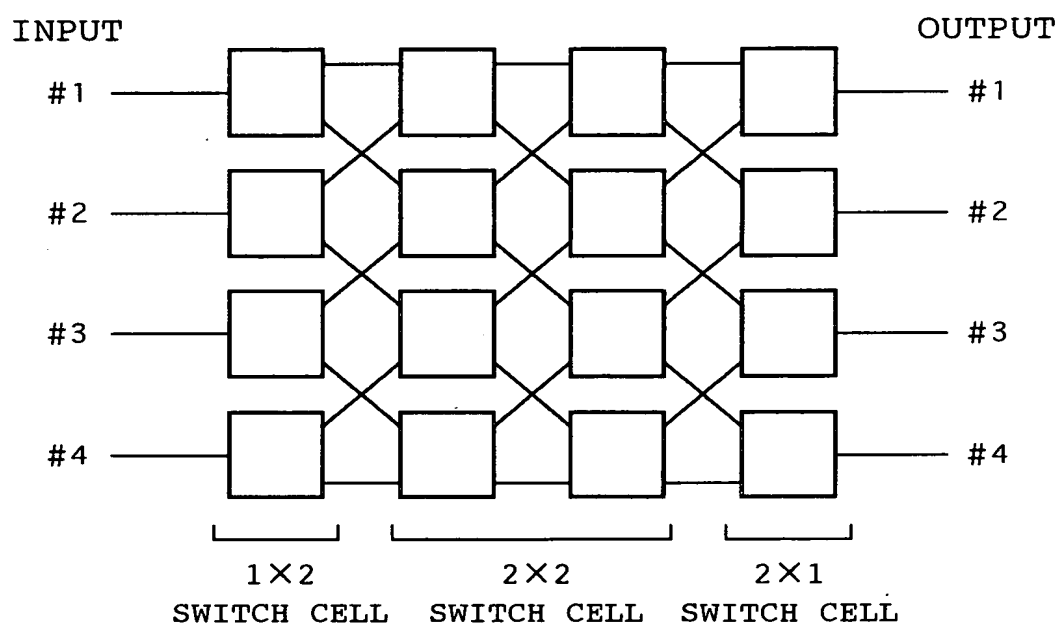
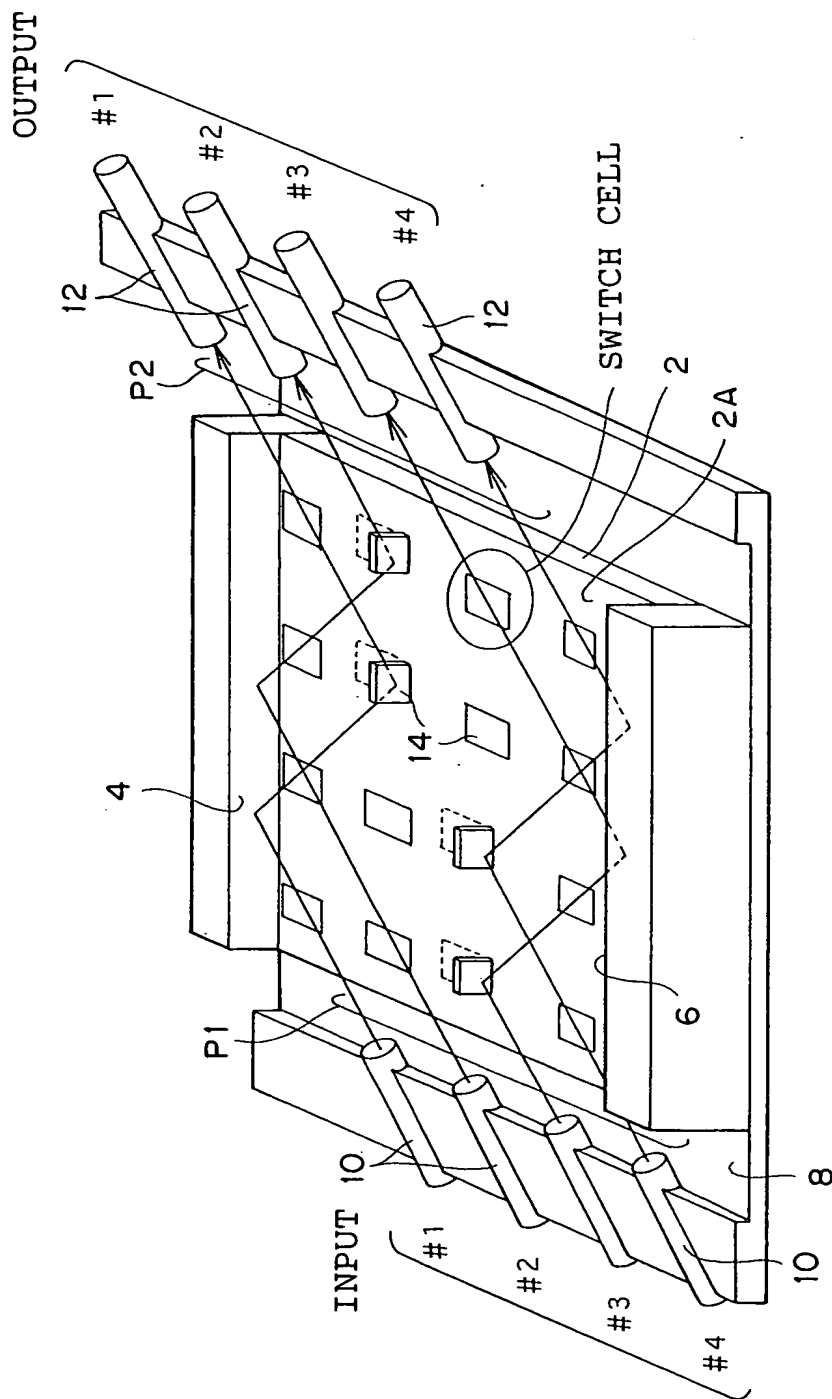
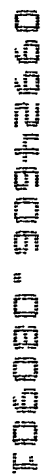


FIG.3



00000000000000000000000000000000



00000000000000000000000000000000

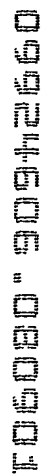


FIG. 5

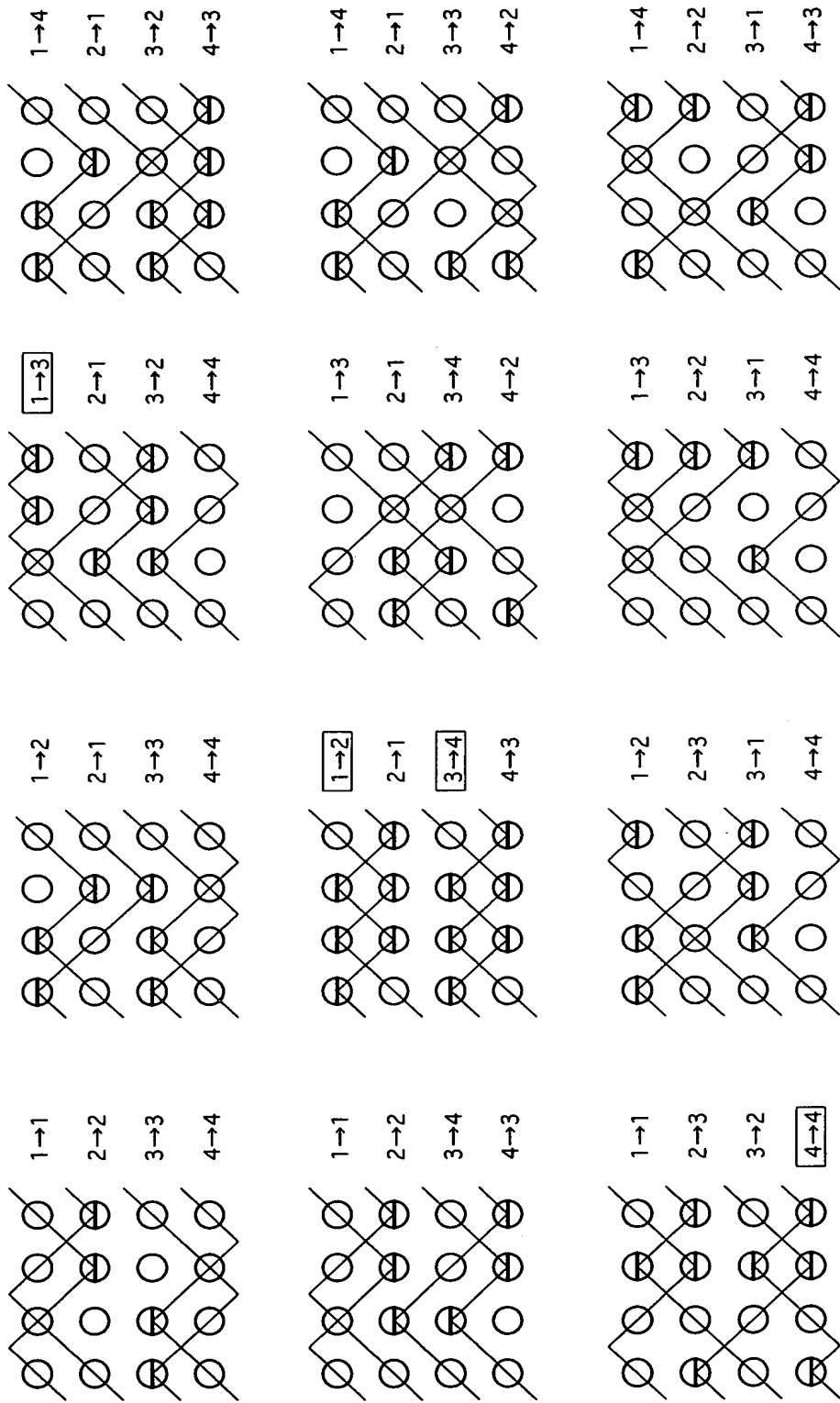
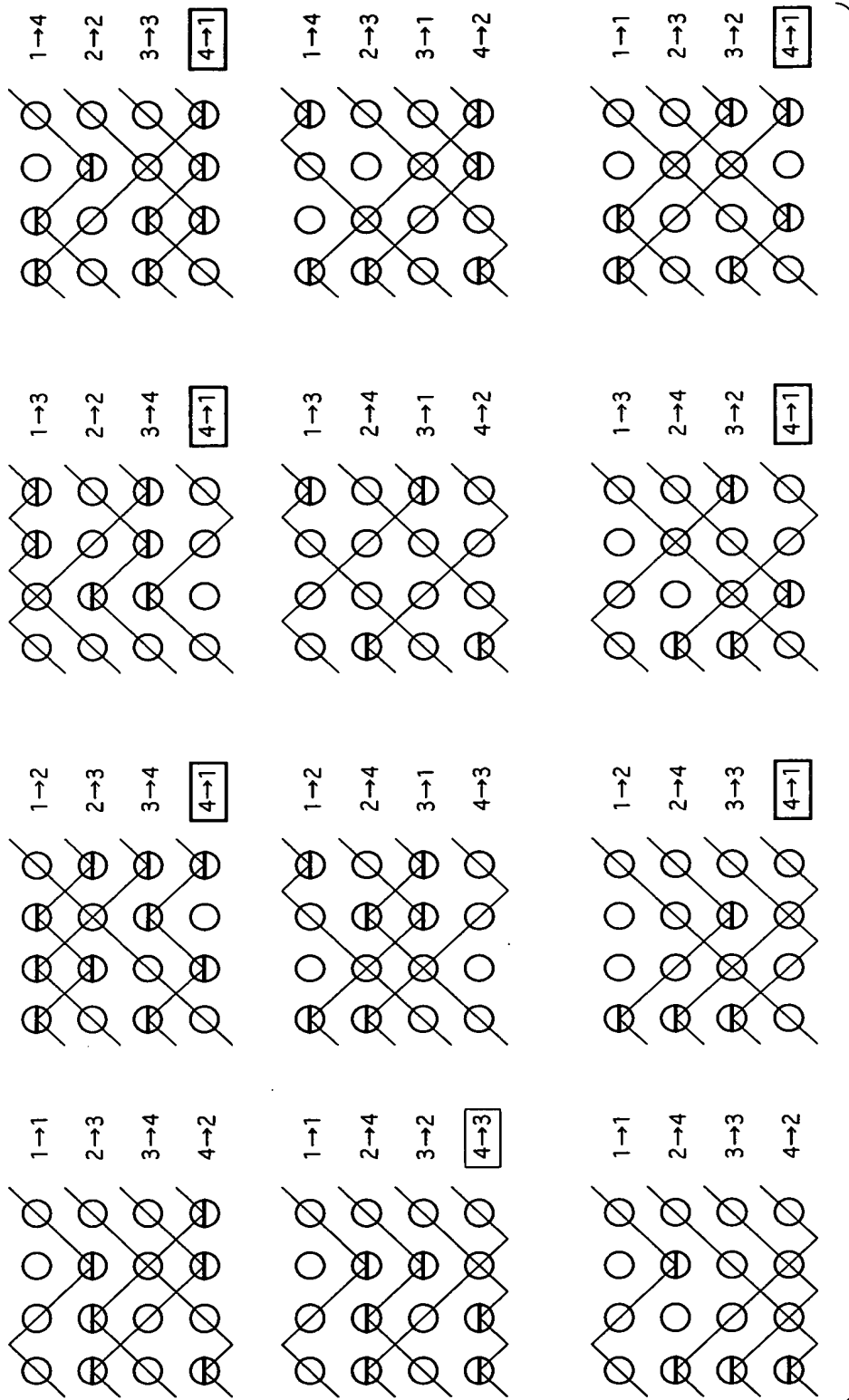
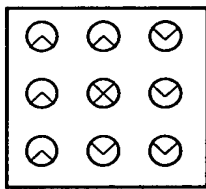
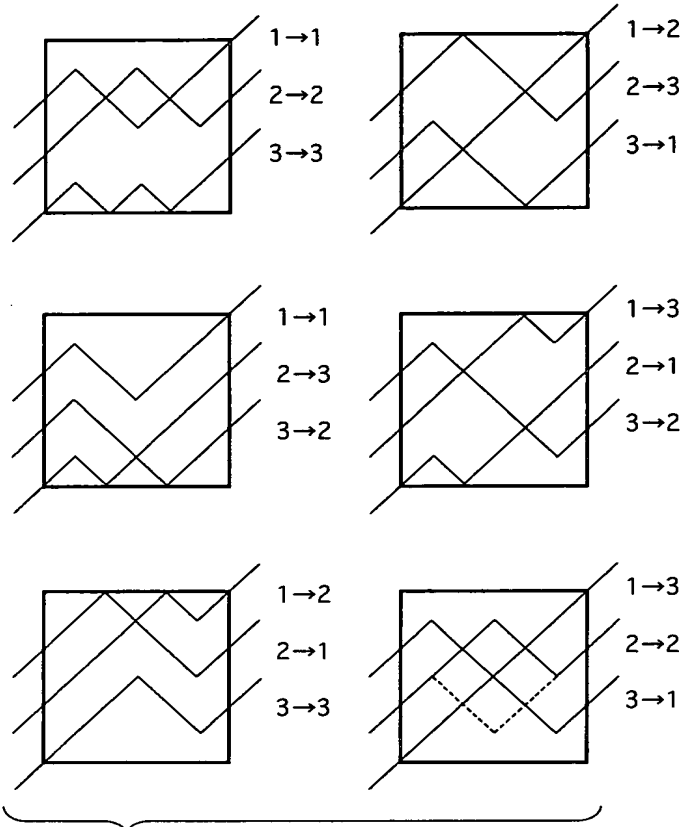


FIG. 6



⊗	⊗	⊗	⊗	SIZE; 4 x 4
⊗	⊗	⊗	⊗	NUMBER OF CELLS; 16
⊗	⊗	⊗	⊗	OPTICAL PATH LENGTH; 4
⊗	⊗	⊗	⊗	NUMBER OF REFLECTIONS; 2/4/0
⊗	⊗	⊗	⊗	KINDS OF MIRRORS; DOWNWARD REFLECTION; 5
⊗	⊗	⊗	⊗	UPWARD REFLECTION; 5
⊗	⊗	⊗	⊗	BIDIRECTIONAL REFLECTION; 6

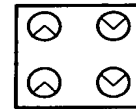
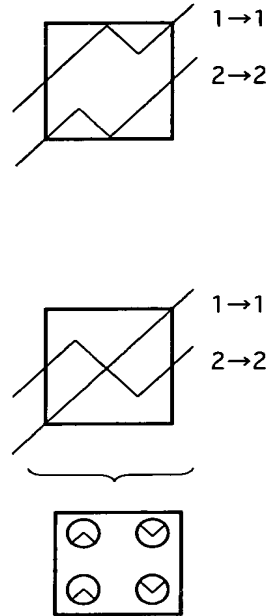
FIG.7A



SIZE;3 x 3
 OPTICAL PATH LENGTH ;3
 NUMBER OF REFLECTIONS;2/4/0
 KINDS OF MIRRORS;UPWARD REFLECTIN;4
 DOWNWARD REFLECTION;4
 BIDIRECTIONAL REFLECTION;1
 NUMBER OF CELLS;9

3 x 3 OPTICAL SWITCH

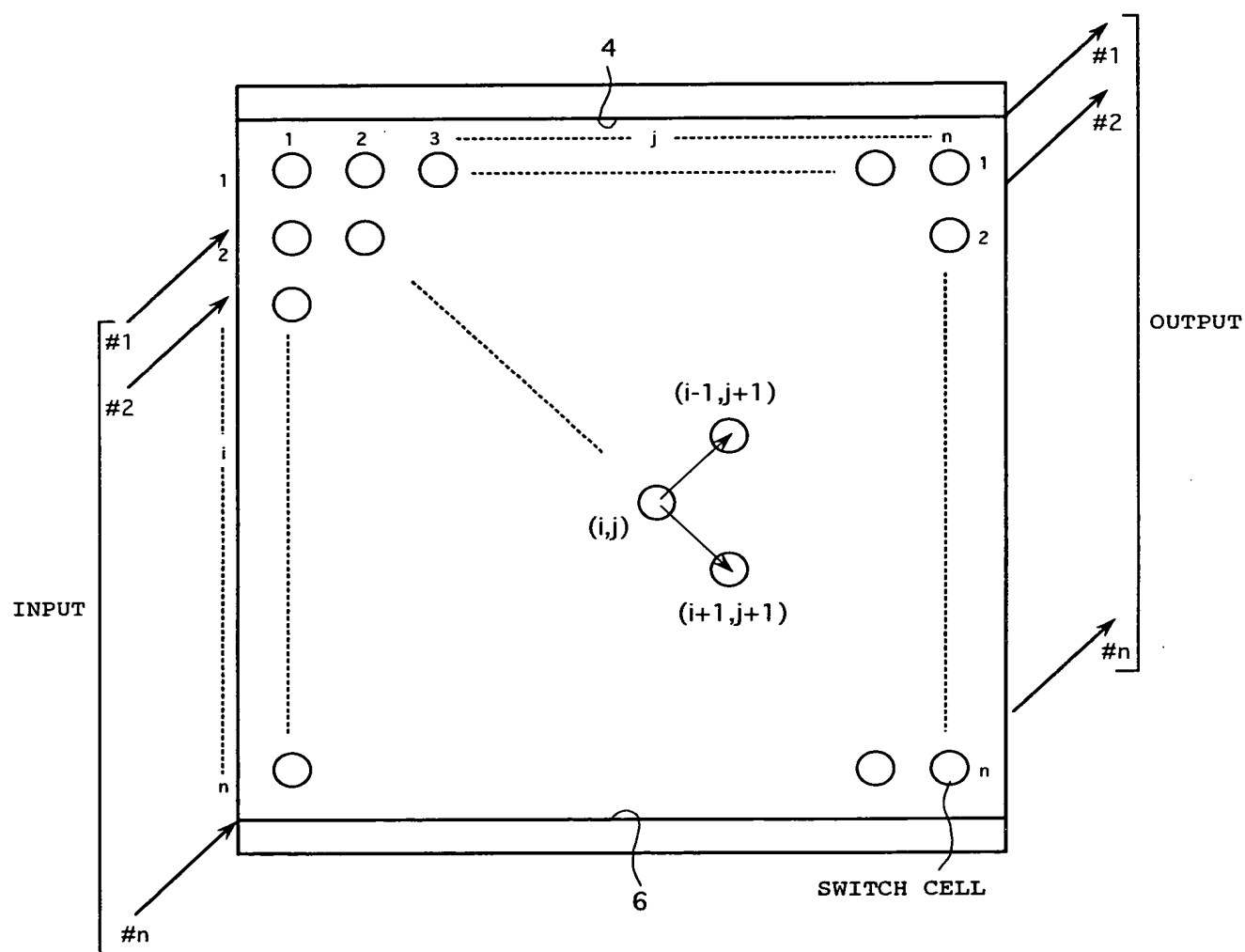
FIG.7B



SIZE;2 x 2
 OPTICAL PATH LENGTH ;2
 NUMBER OF REFLECTIONS;2/1
 KINDS OF MIRRORS;UPWARD REFLECTIN;2
 DOWNWARD REFLECTION;2
 NUMBER OF CELLS;4

2 x 2 OPTICAL SWITCH

FIG.8



NUMBER OF SWITCH CELLIS;

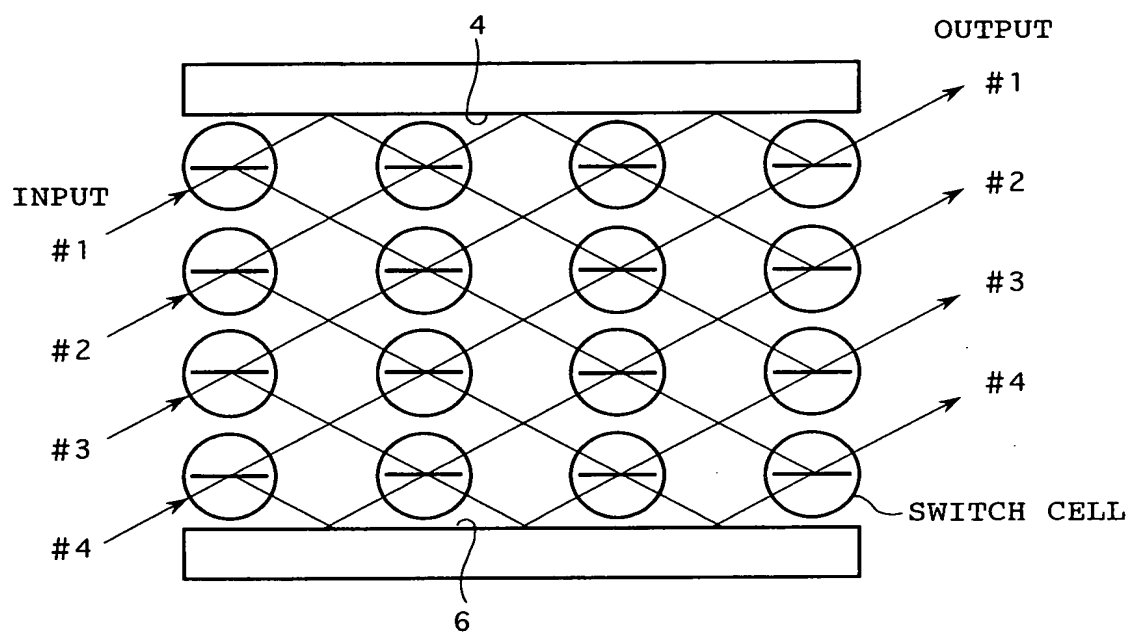
UPWARD REFLECTION; $n+1$

DOWNWARD REFLECTION; $n+1$

BIDIRECTIONAL REFLECTION; n^2-2n-2

TOTAL NUMBER; n^2

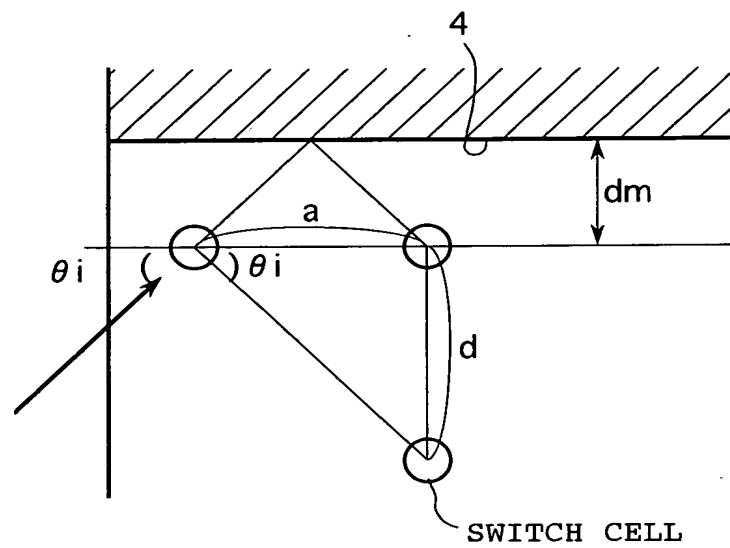
FIG.9



ANGLE OF INCIDENCE; 30°

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FIG.10



$$d = a \cdot \tan \theta_i$$

$$dm = 1/2 \cdot a \cdot \tan \theta_i$$

FIG. 11

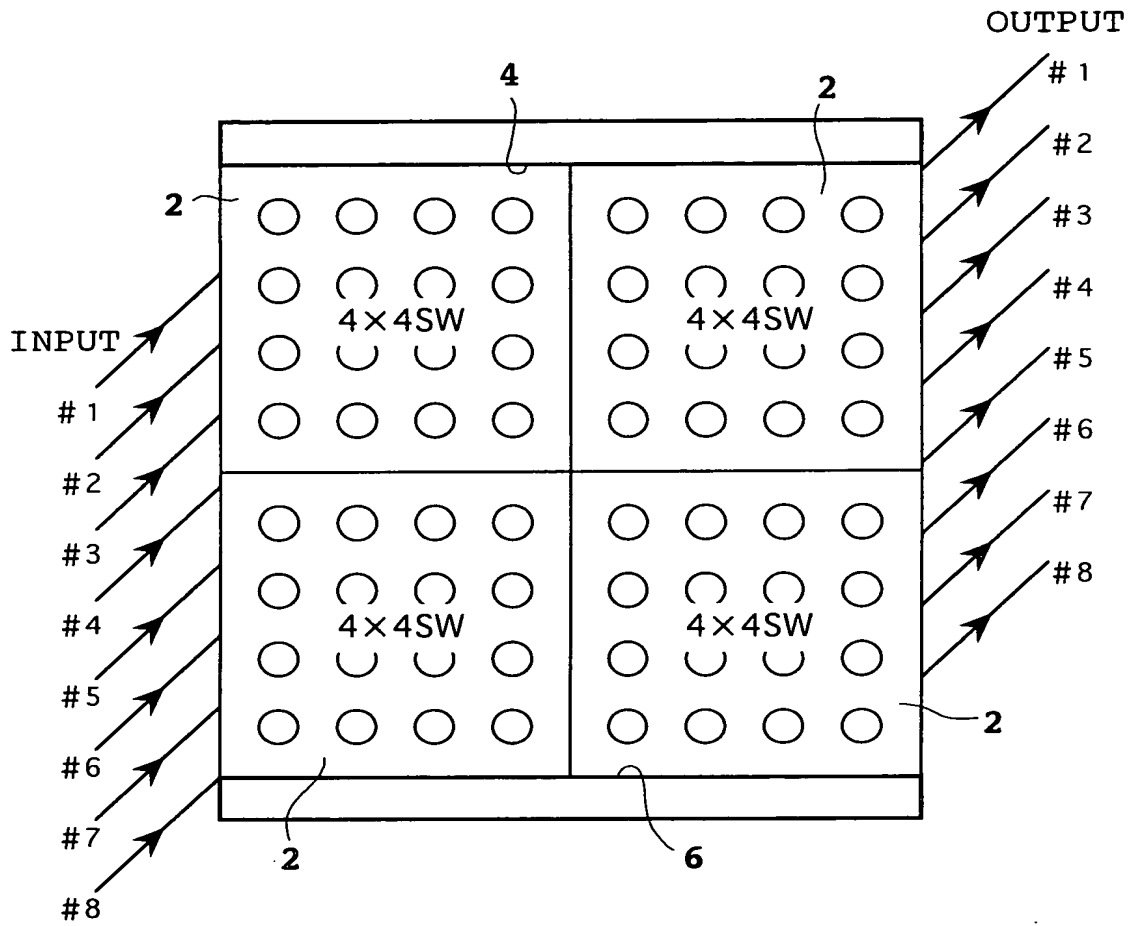


FIG.12A

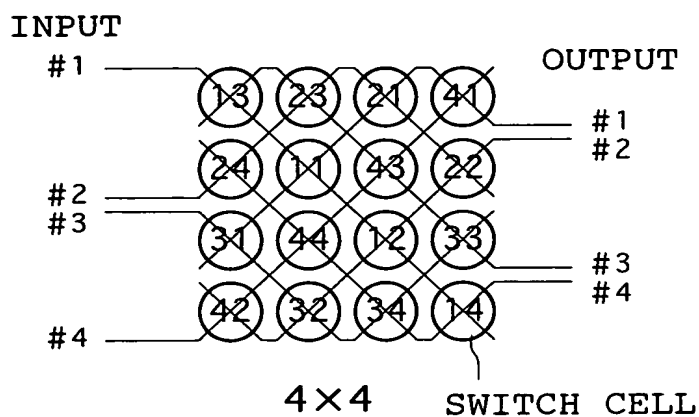


FIG.12B

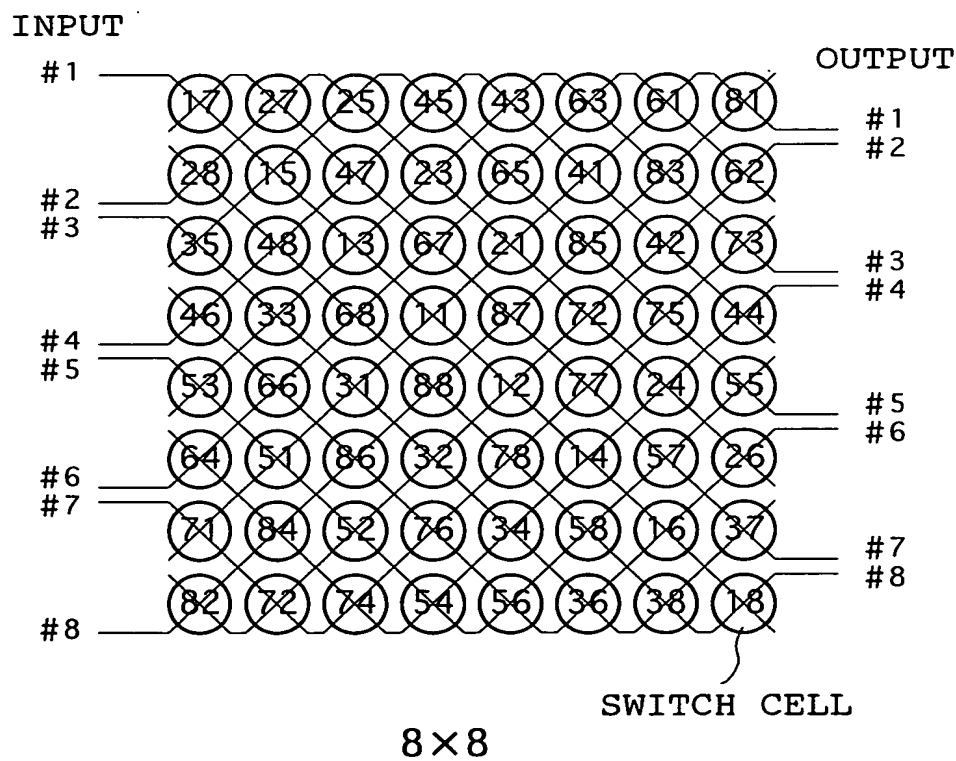


FIG.13A

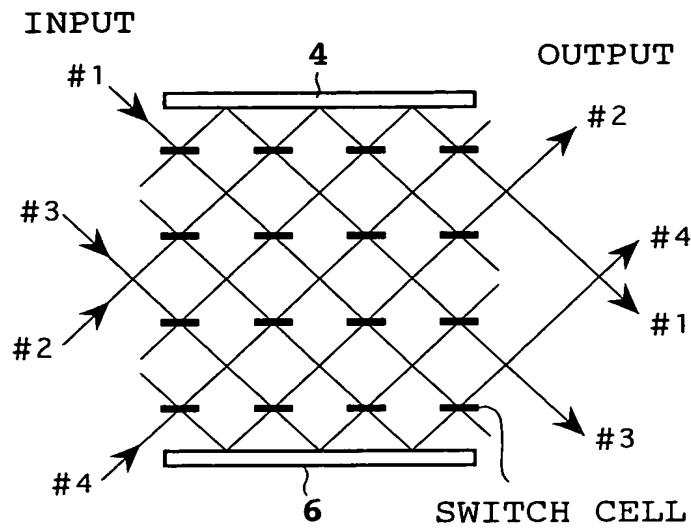


FIG.13B

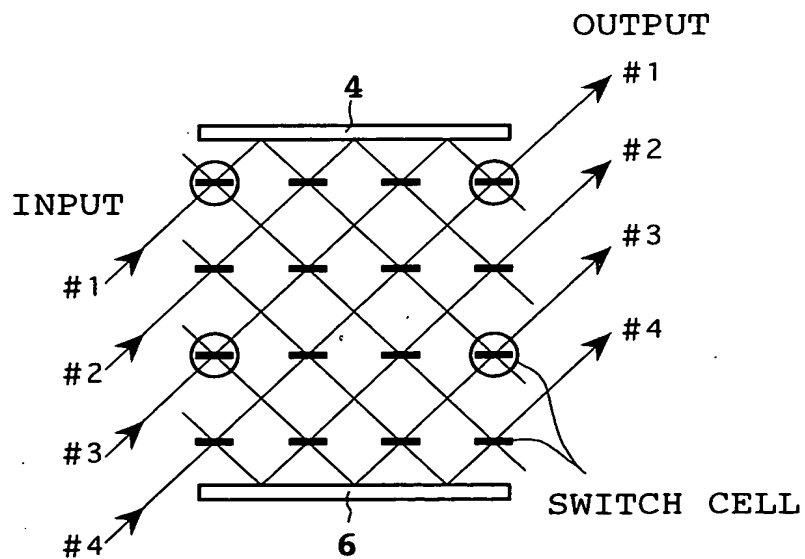


FIG.1 4A

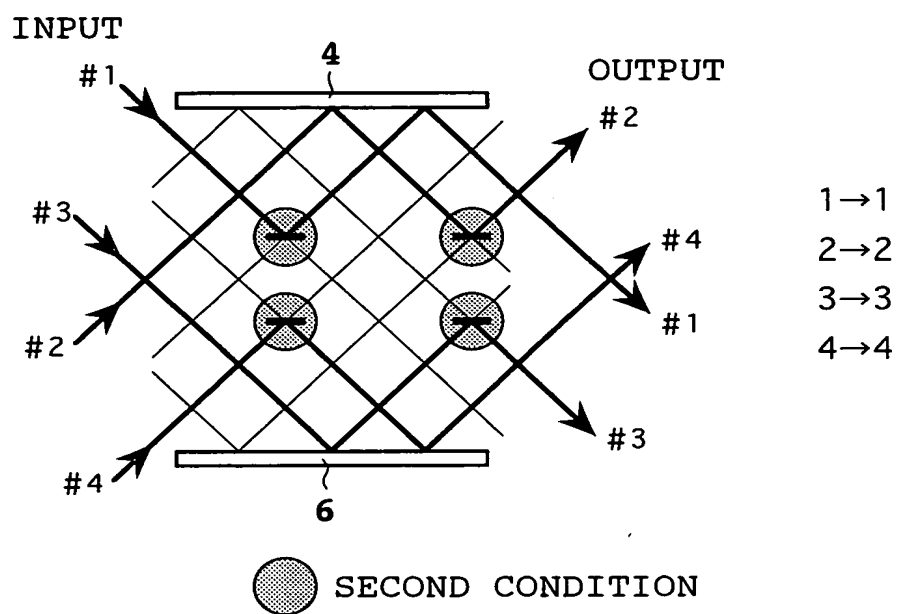


FIG.1 4B

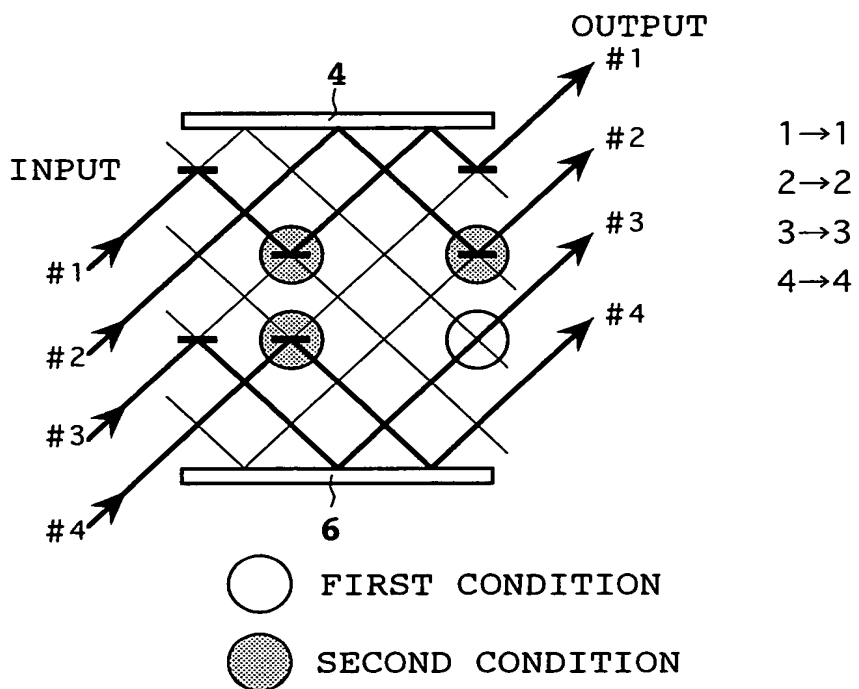


FIG.15

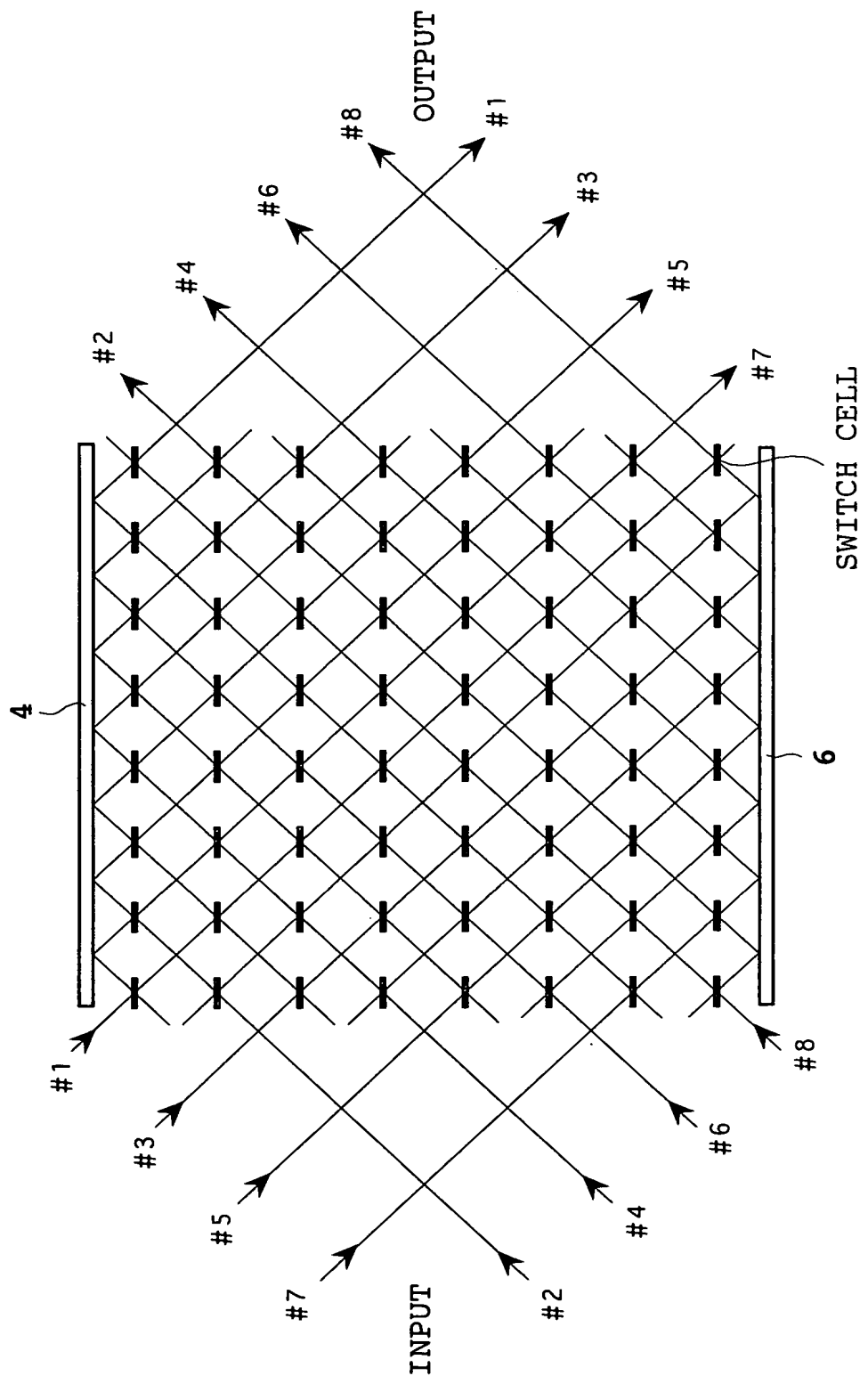


FIG. 16

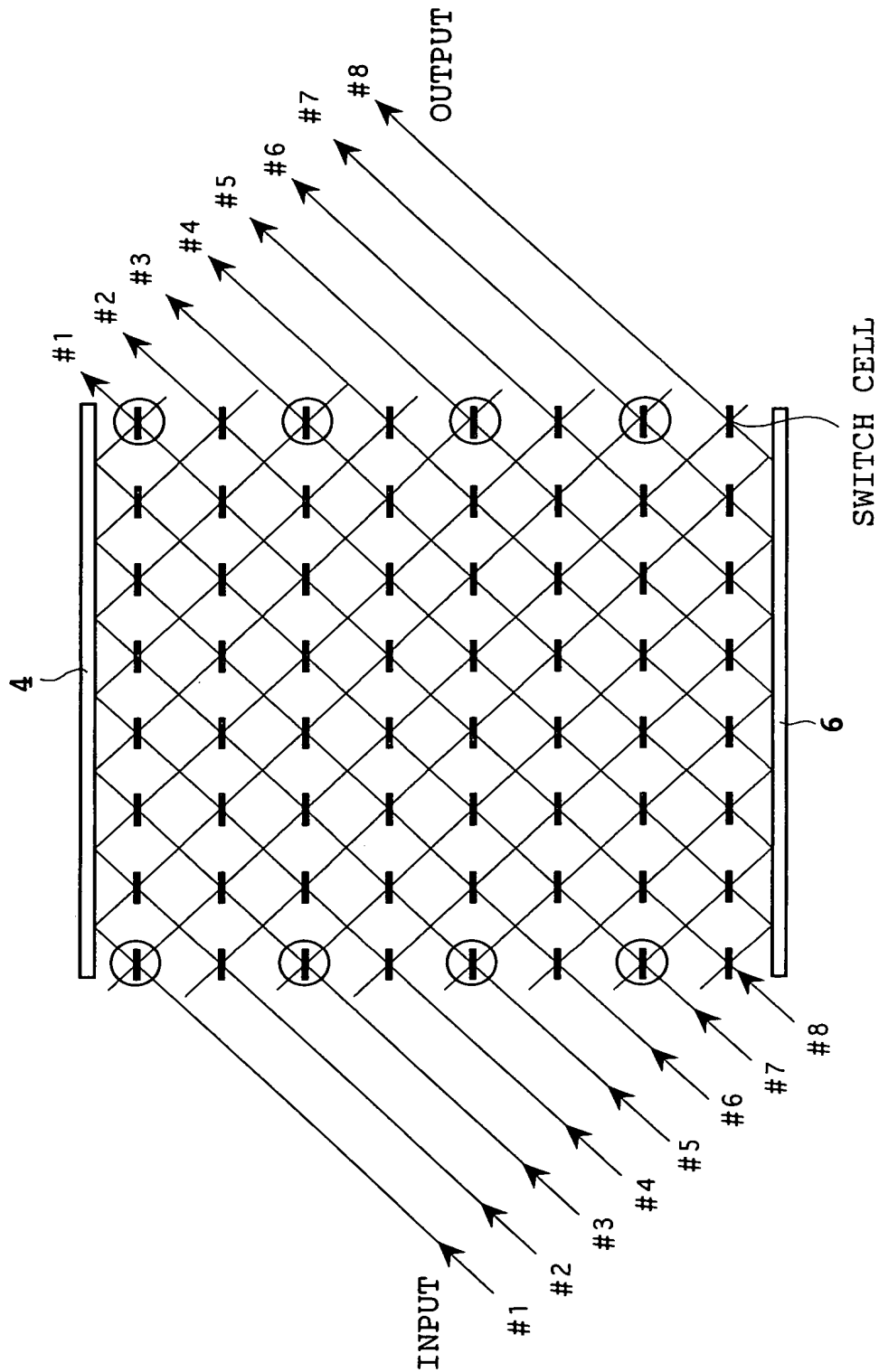


FIG.17A

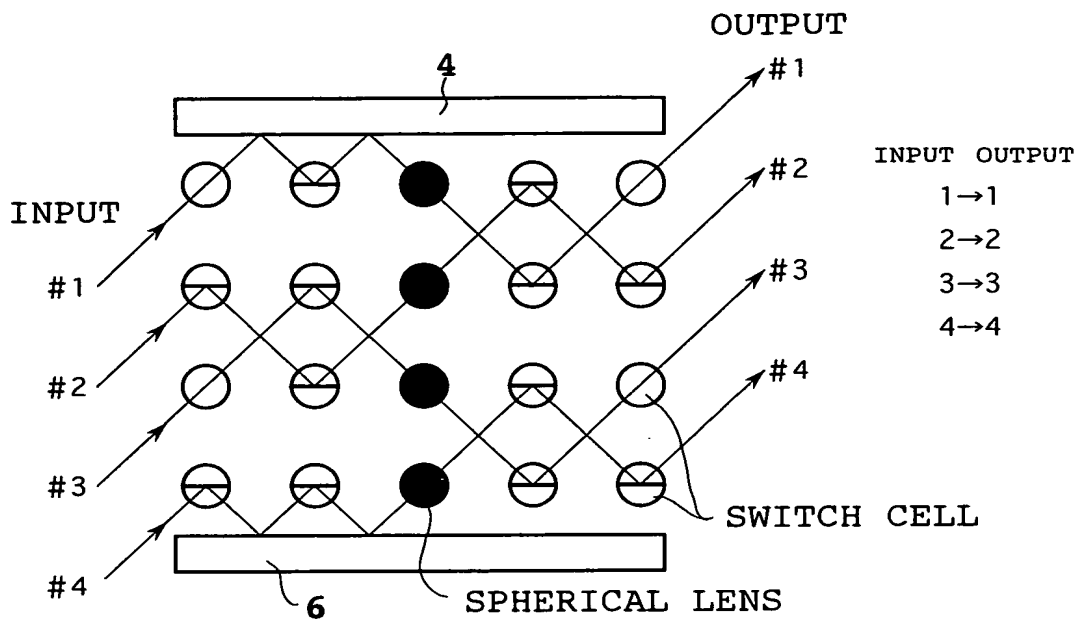


FIG.17B

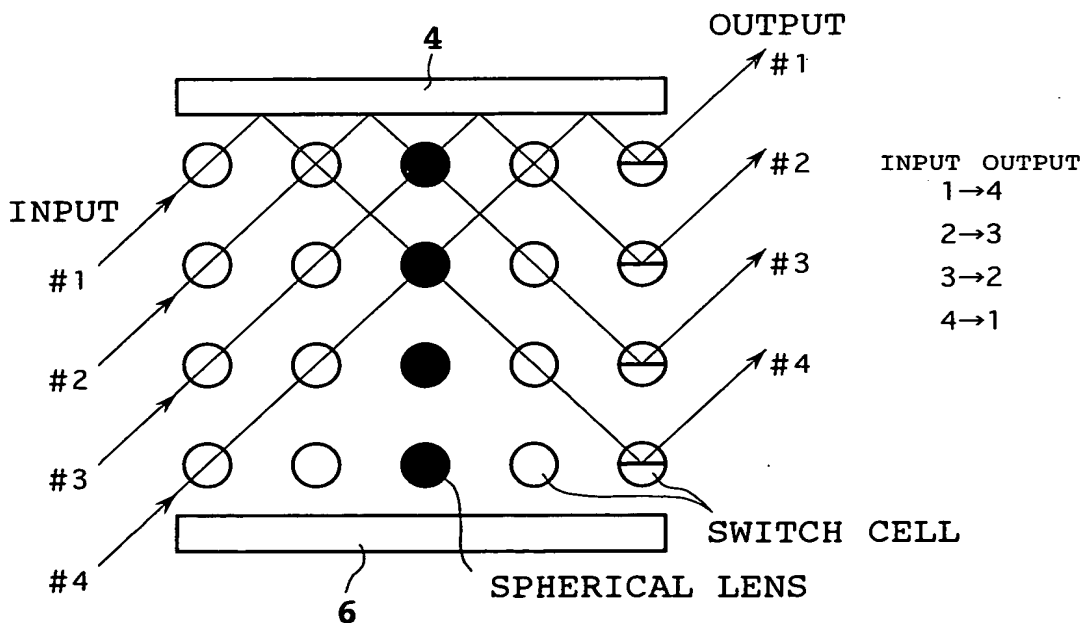
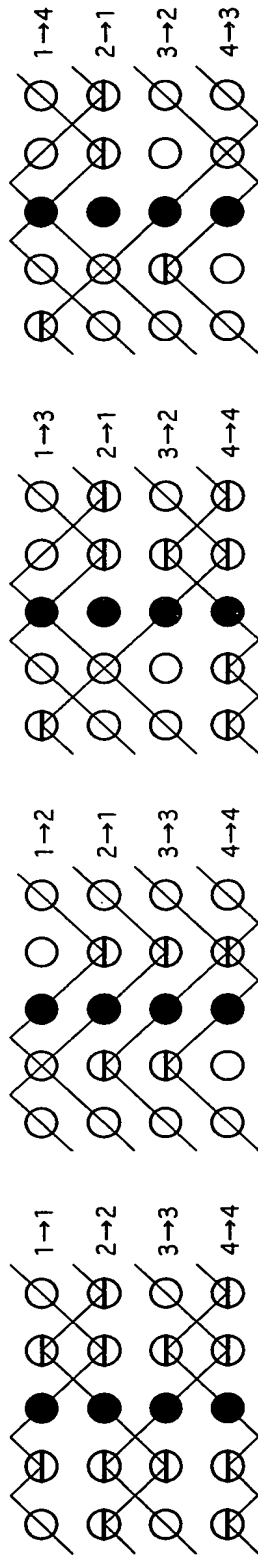
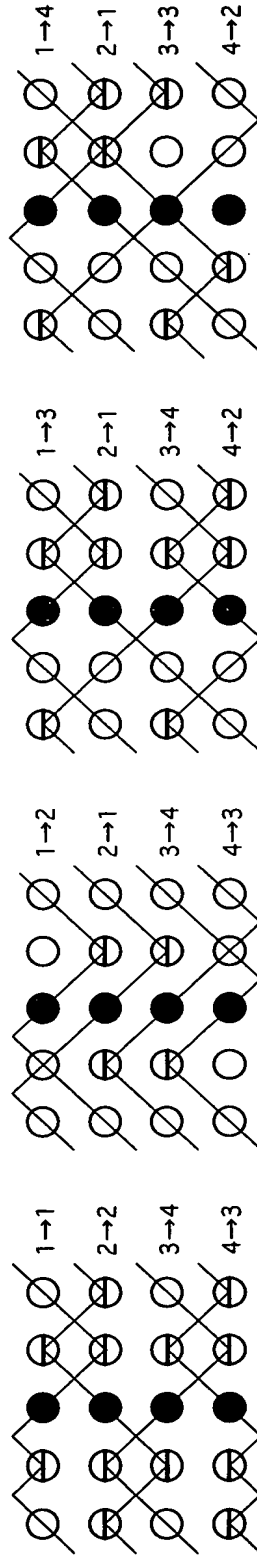


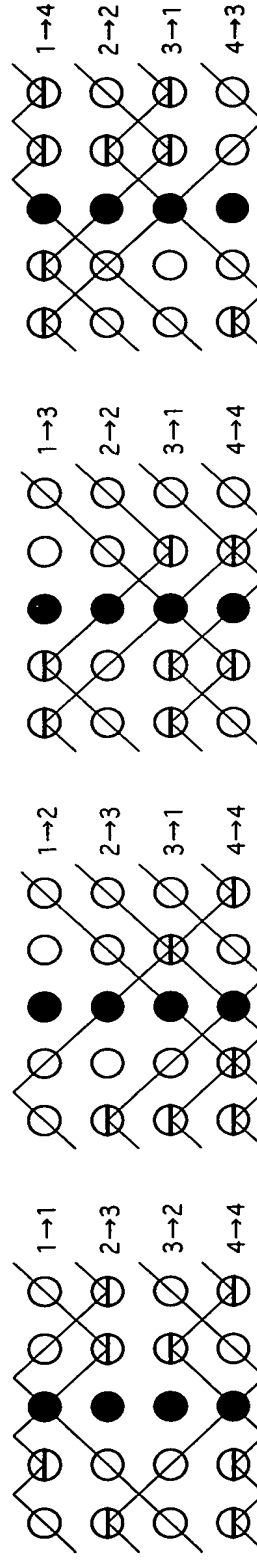
FIG. 18



SIMULTANEOUS BIDIRECTIONAL
REFLECTION; ONE CELL



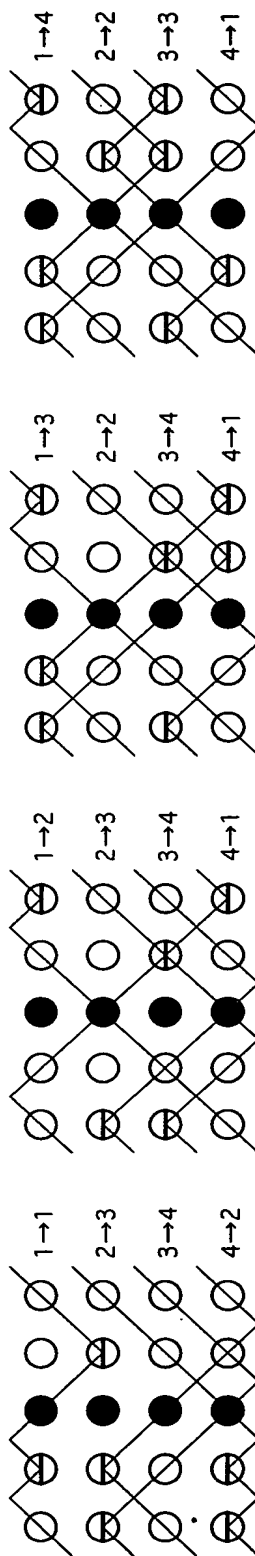
SIMULTANEOUS BIDIRECTIONAL
REFLECTION; ONE CELL



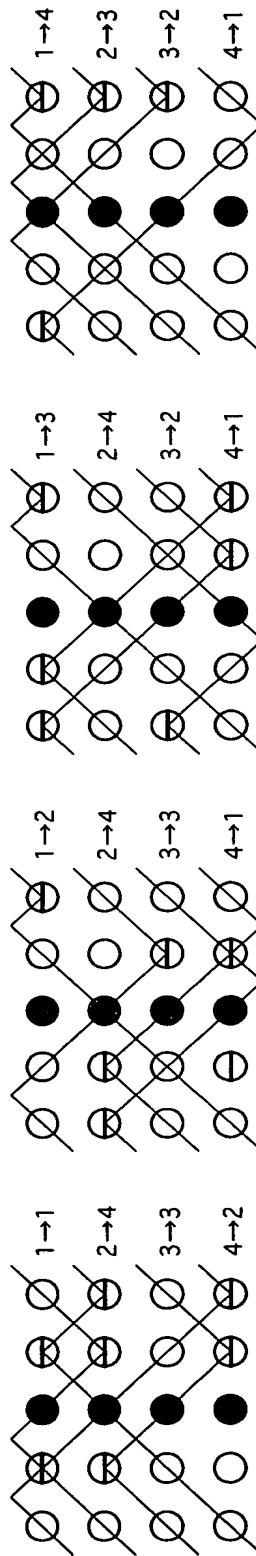
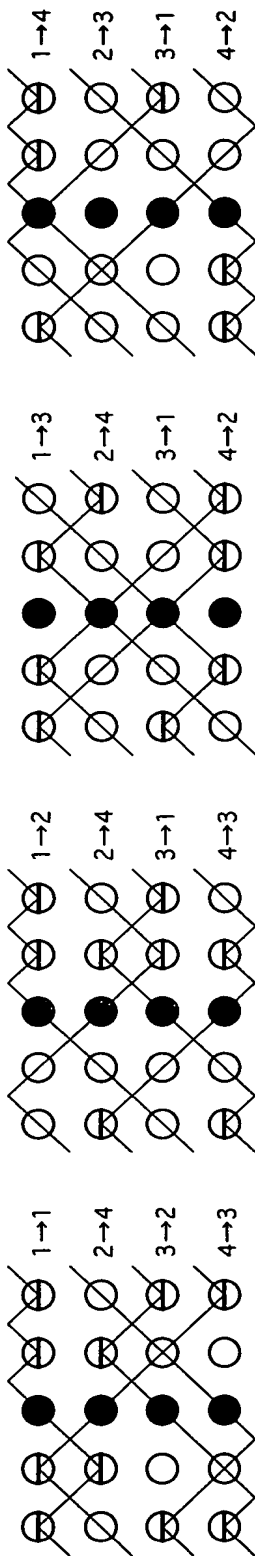
SIMULTANEOUS BIDIRECTIONAL
REFLECTION; TWO CELLS

SIMULTANEOUS BIDIRECTIONAL
REFLECTION; ONE CELL

FIG.19



SIMULTANEOUS BIDIRECTIONAL REFLECTION; ONE CELL



SIMULTANEOUS BIDIRECTIONAL REFLECTION; ONE CELL

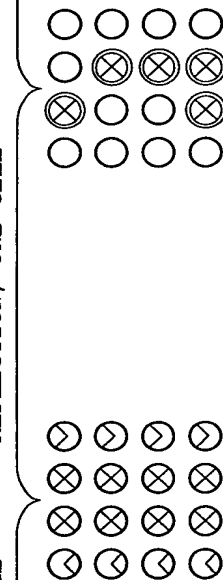
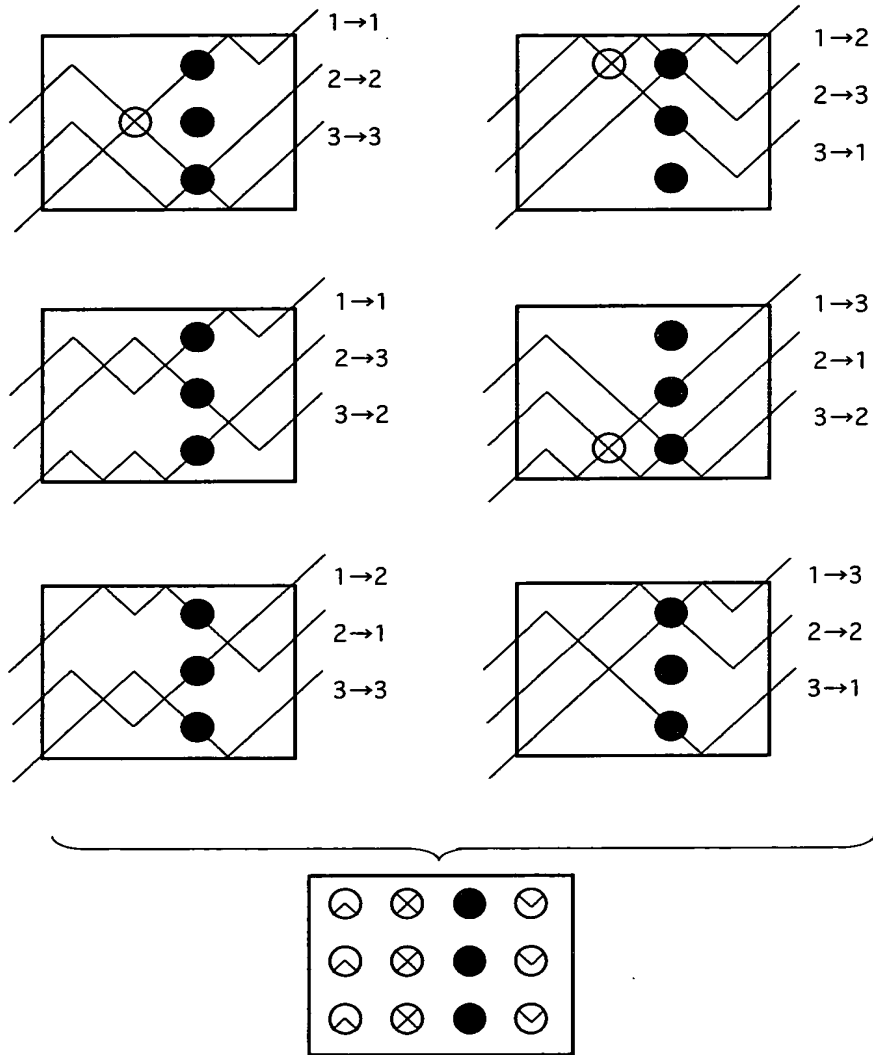


FIG.20



⊗ SIMULTANEOUS BIDIRECTIONAL REFLECTION MIRROR

FIG.21

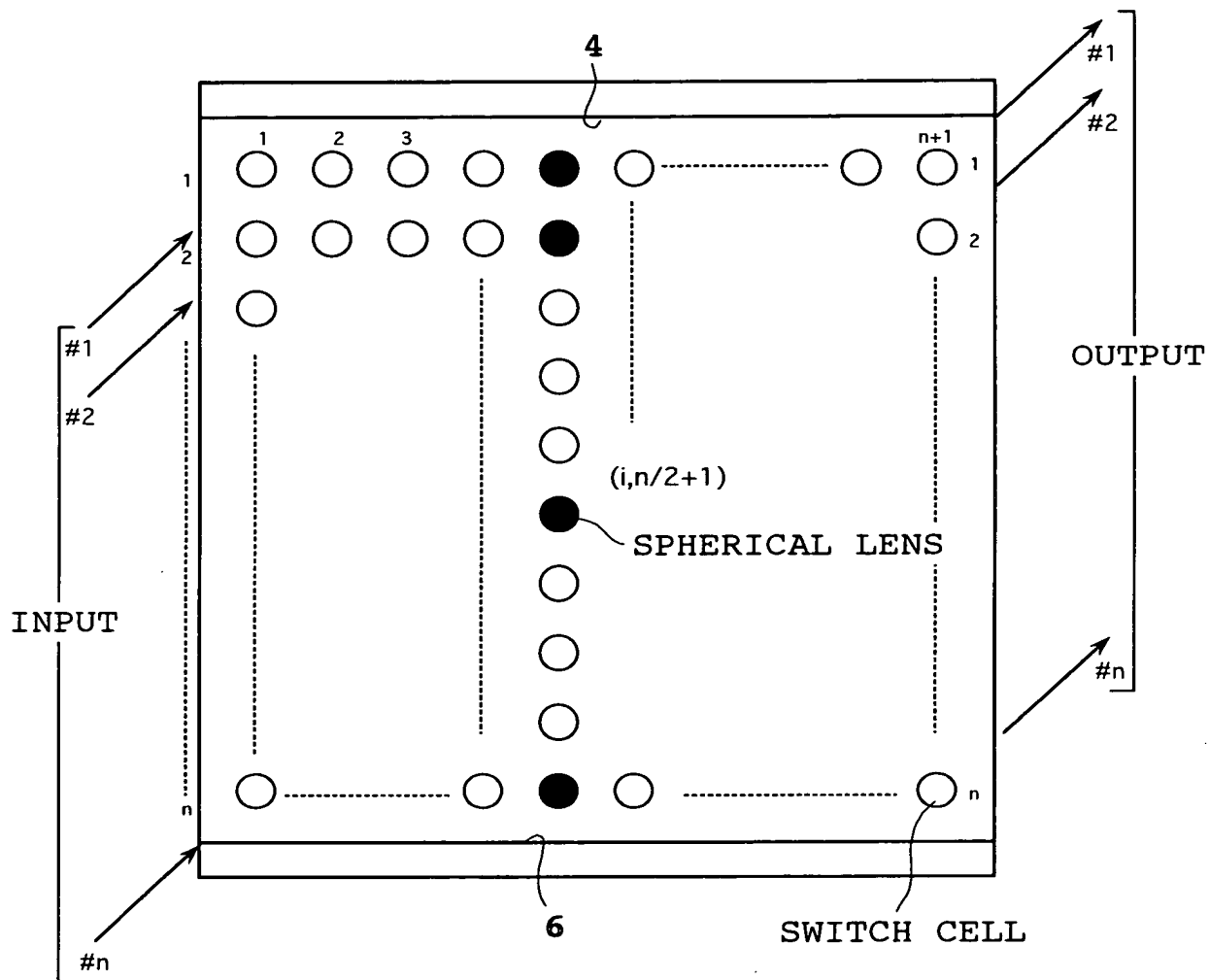


FIG. 21

FIG.22

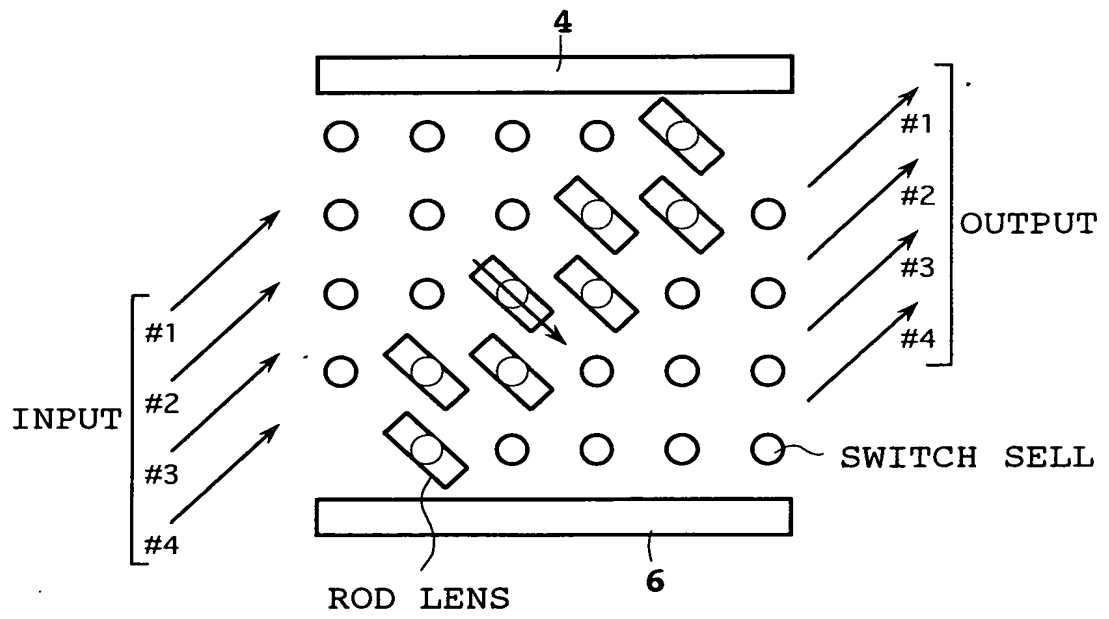


FIG.23

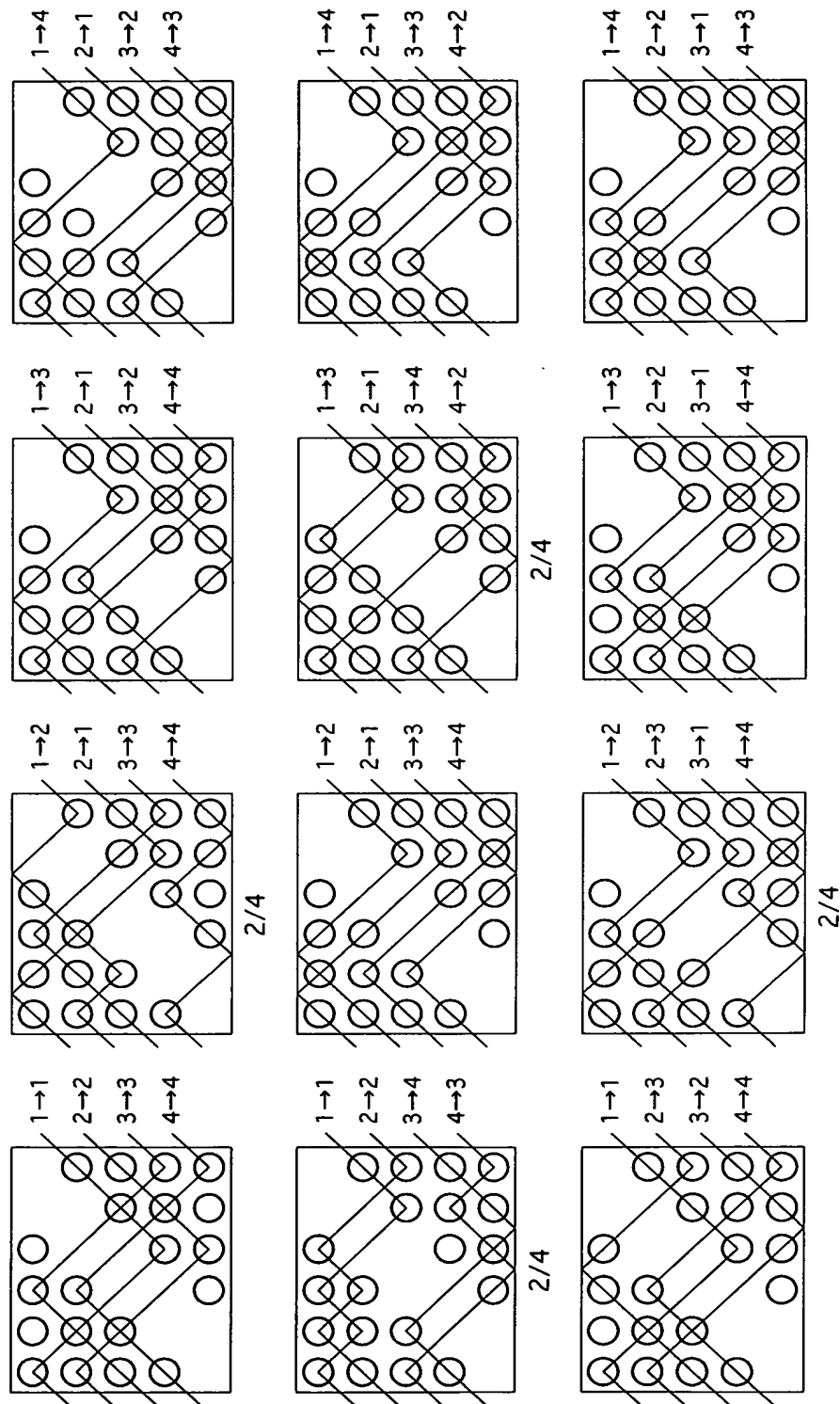


FIG. 24

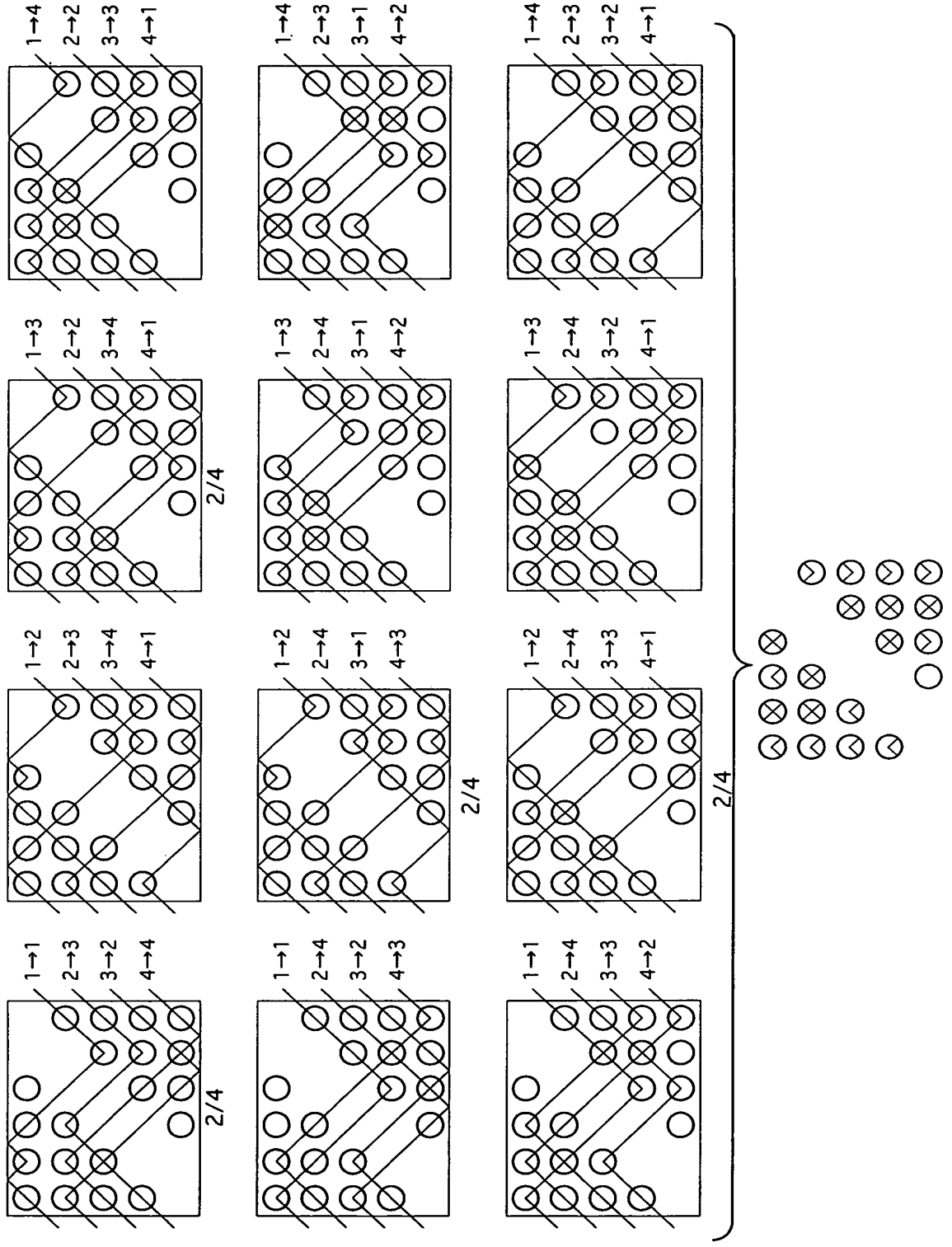


FIG.25

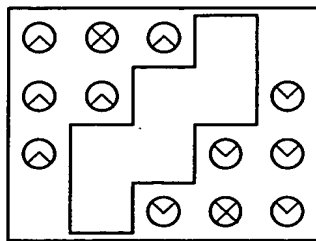
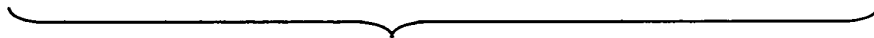
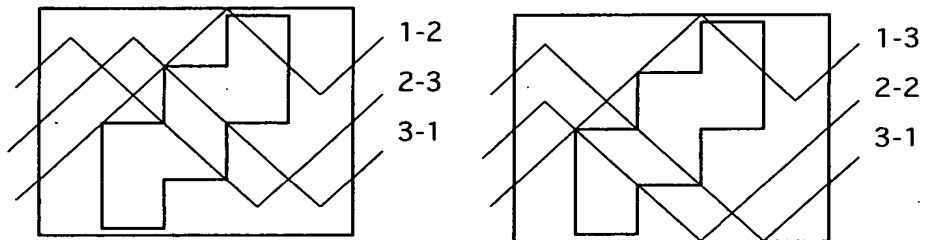
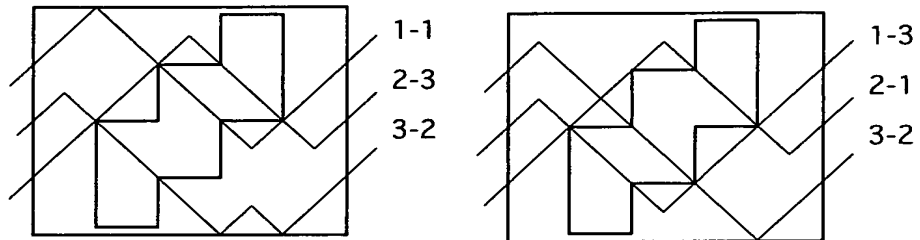
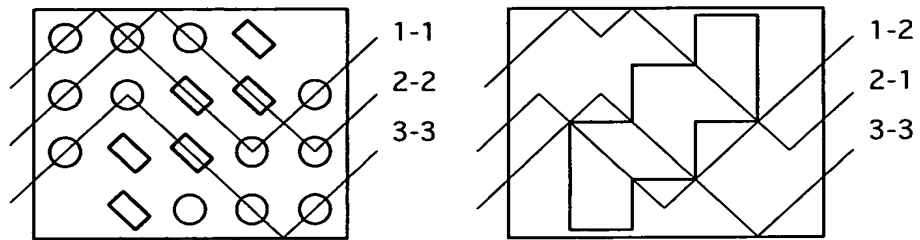
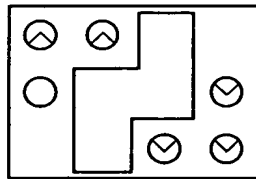
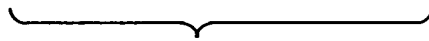
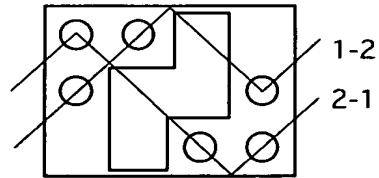
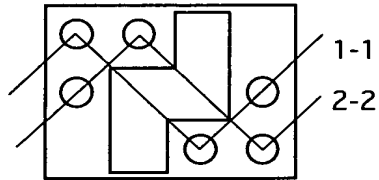


FIG.26



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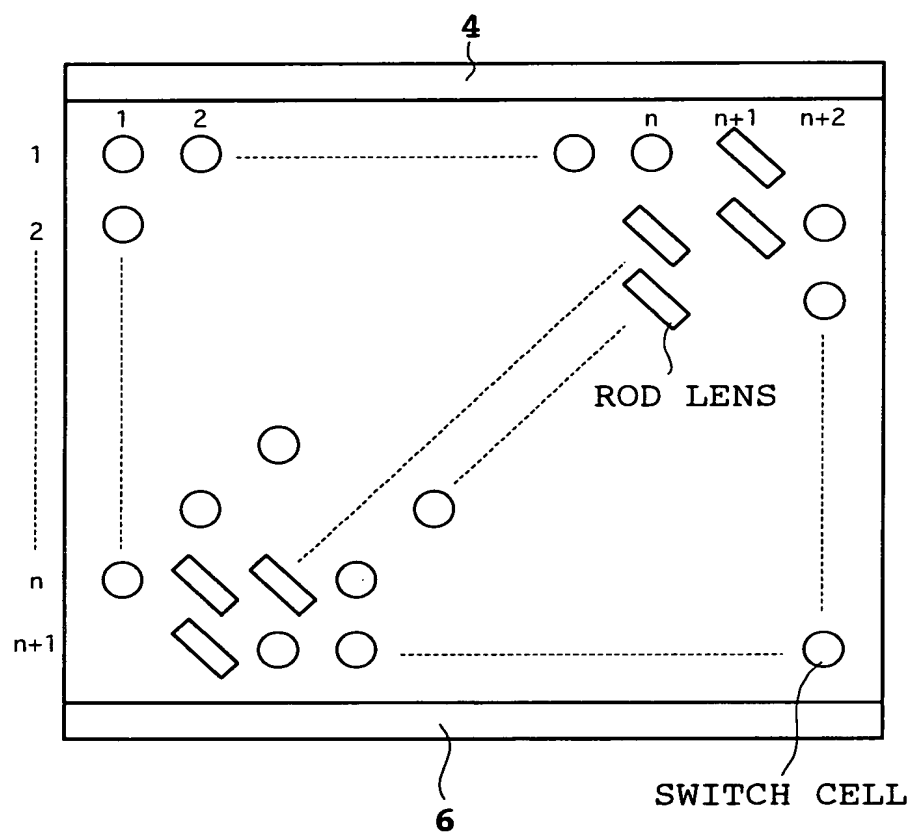


FIG.28

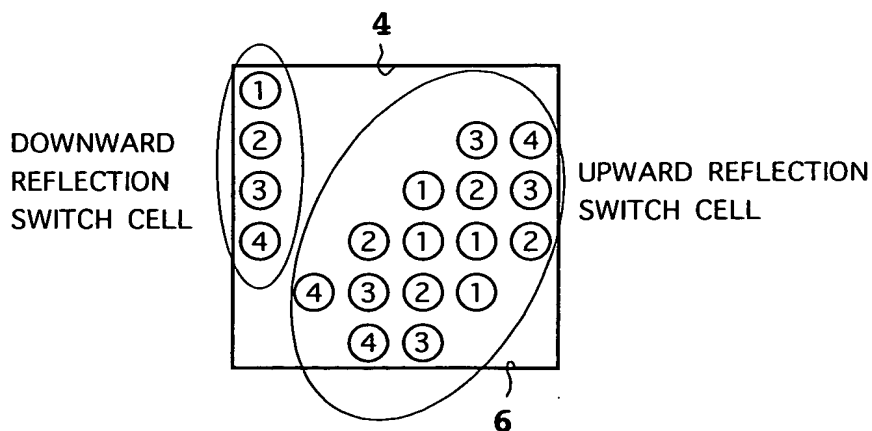
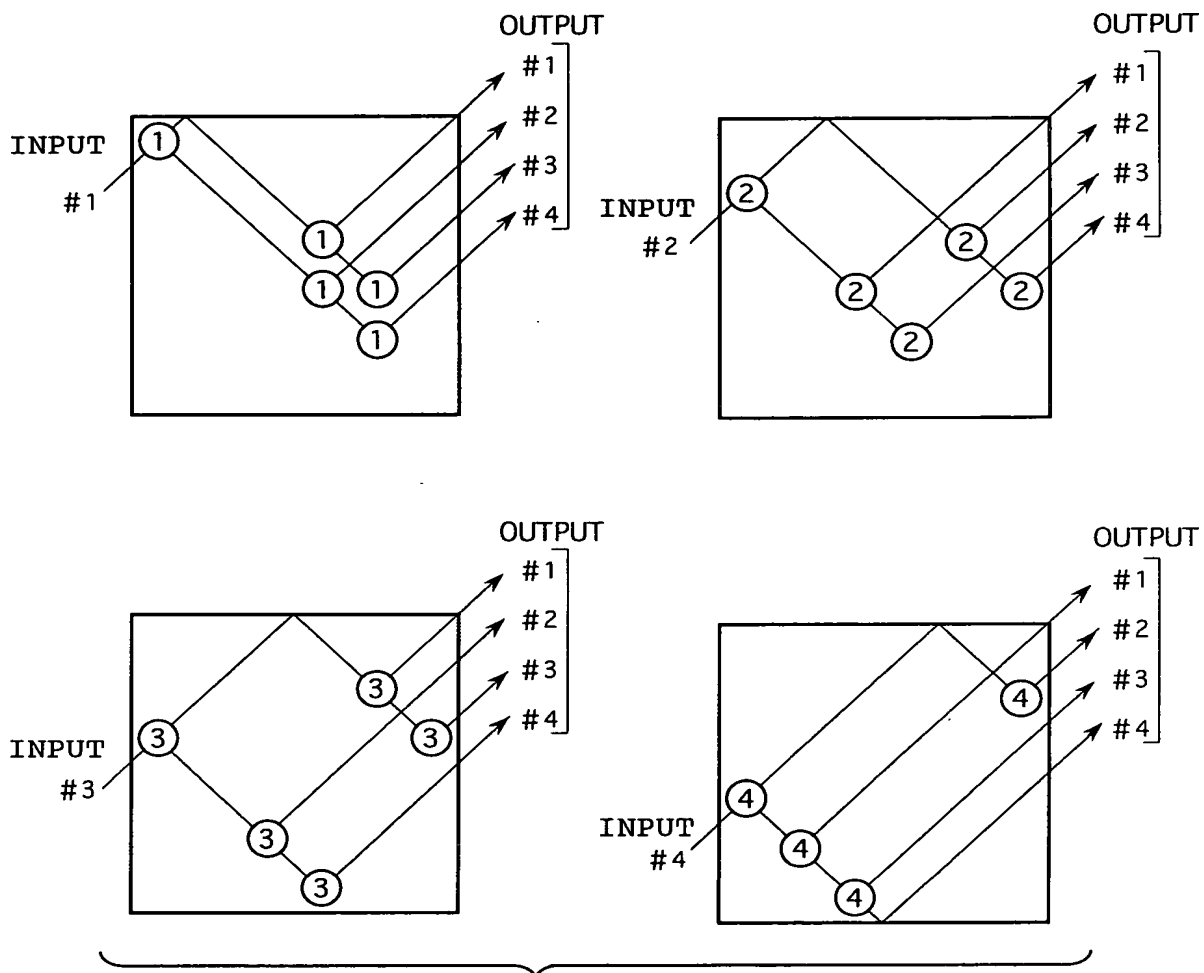
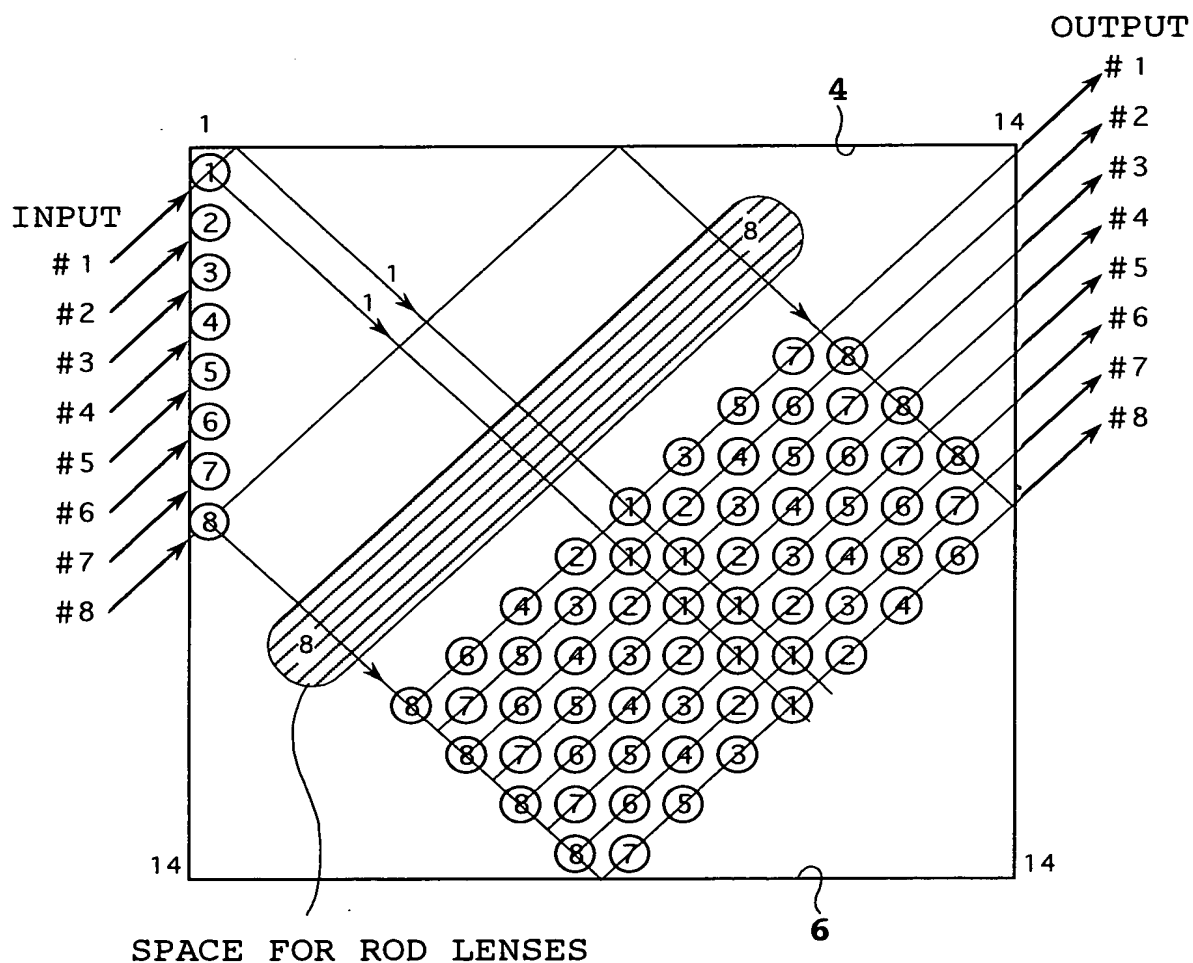


FIG.29



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FIG.30

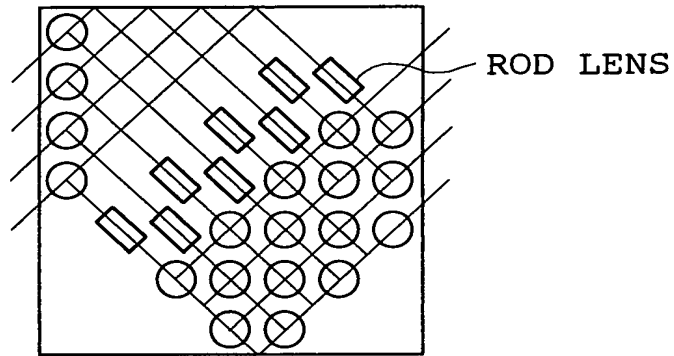
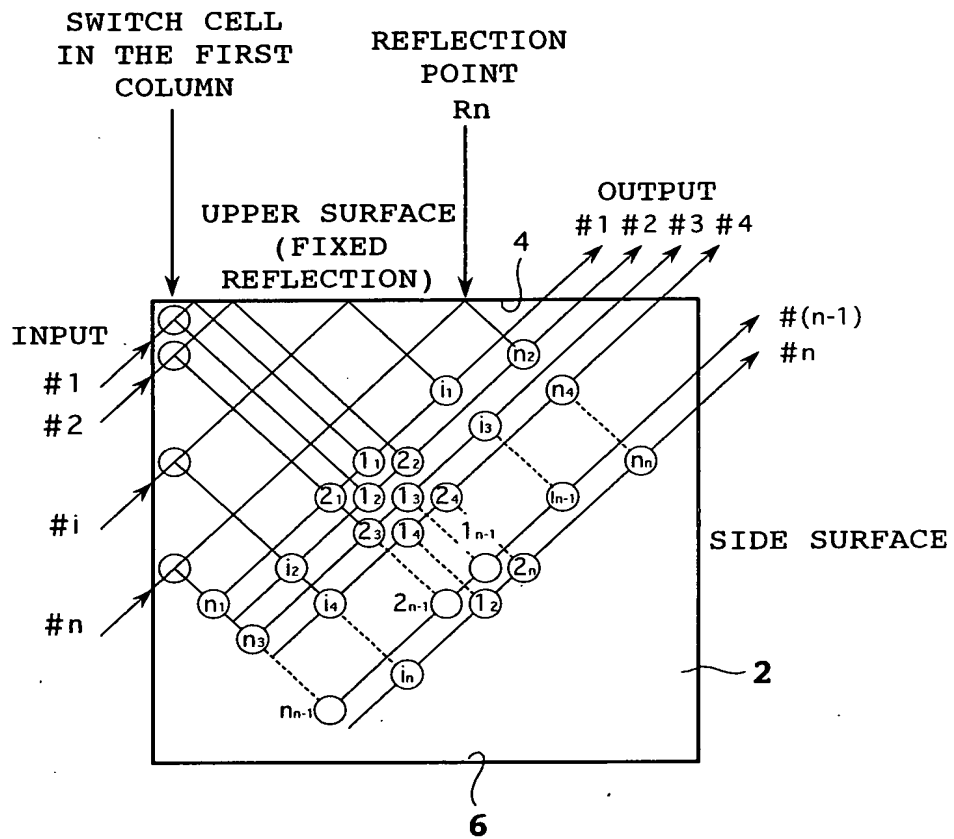


FIG.31



①_n : UPWARD REFLECTION SWITCH CELL FOR
CONNECTING INPUT CHANNEL #i
TO OUTPUT CHANNEL #n

FIG.32

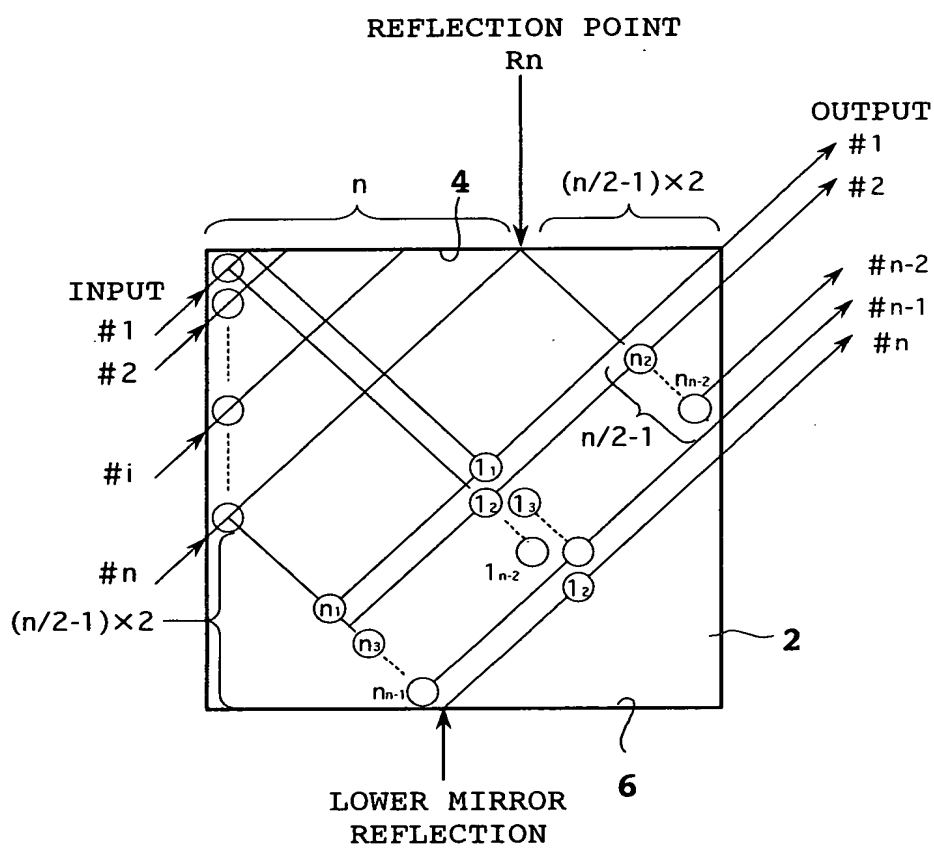


FIG. 32

FIG. 33

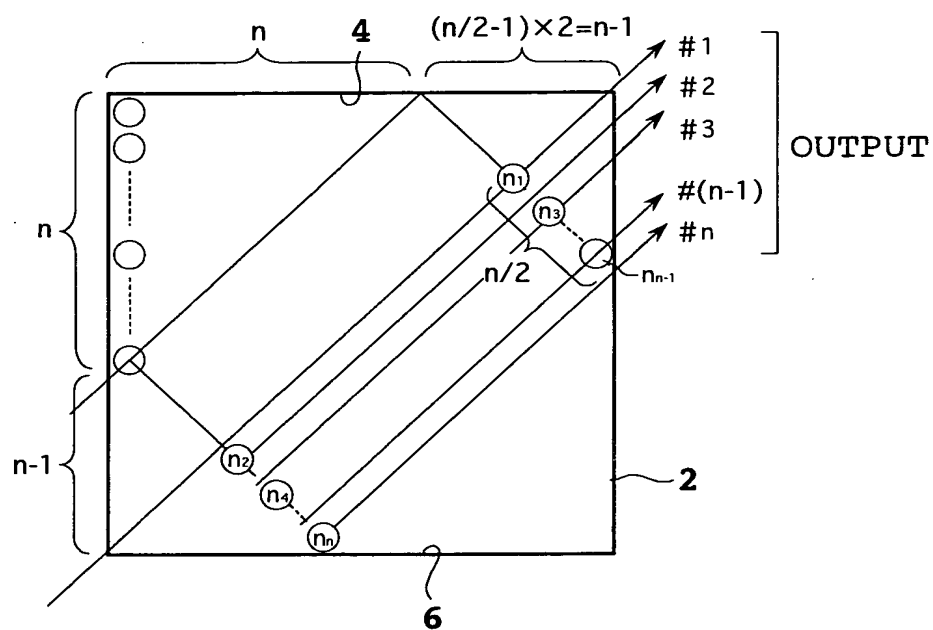


FIG.34

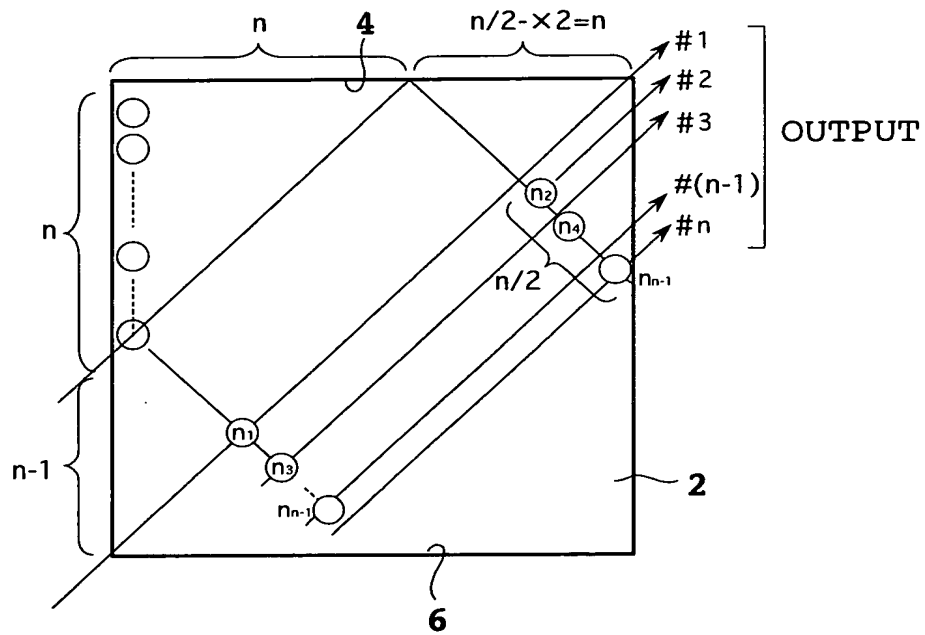


FIG.35

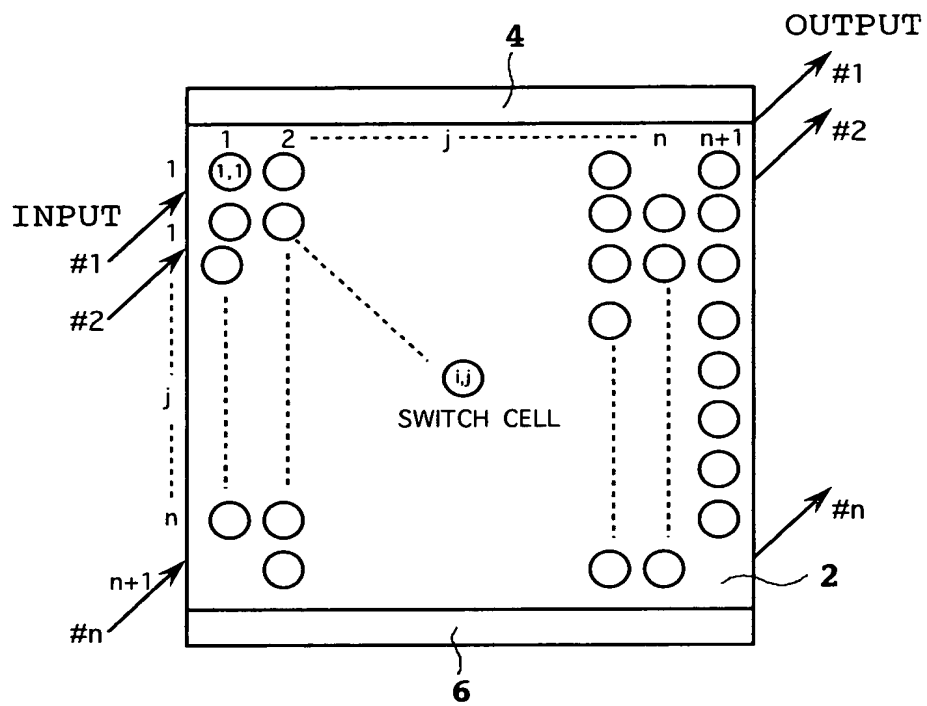


FIG.36

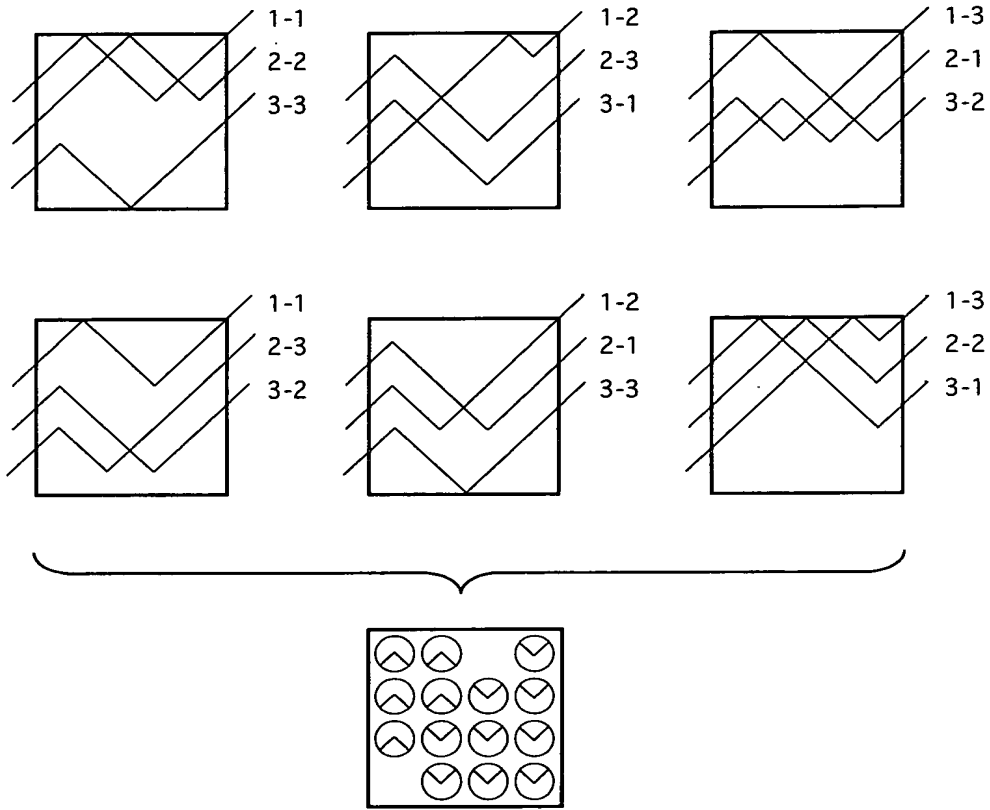
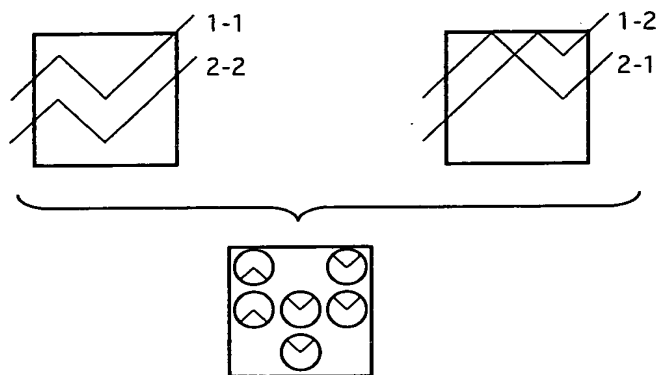


FIG.37



2 x 2 OPTICAL SWITCH

SIZE; 3 x 3

OPTICAL PATH LENGTH; 3

NUMBER OF CELLS; 6

NUMBER OF UPWARD REFLECTION MIRRORS; 4

NUMBER OF DOWNWARD REFLECTION MIRRORS; 2

NUMBER OF REFLECTIONS ; ALWAYS 2

FIG.38

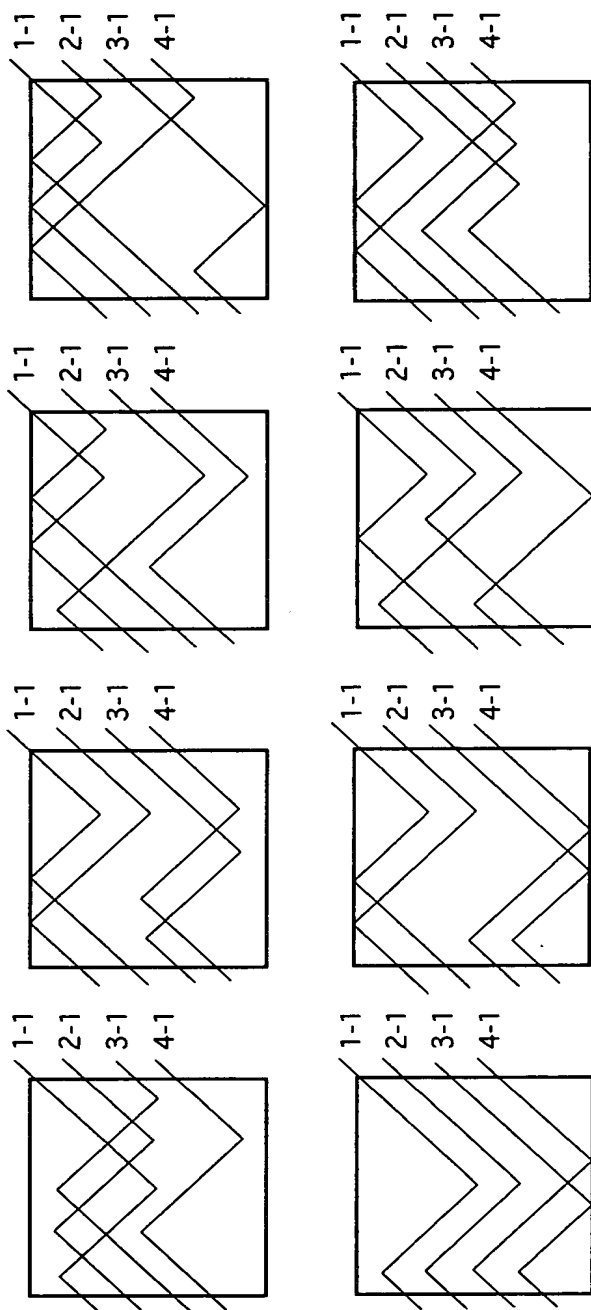


FIG. 39

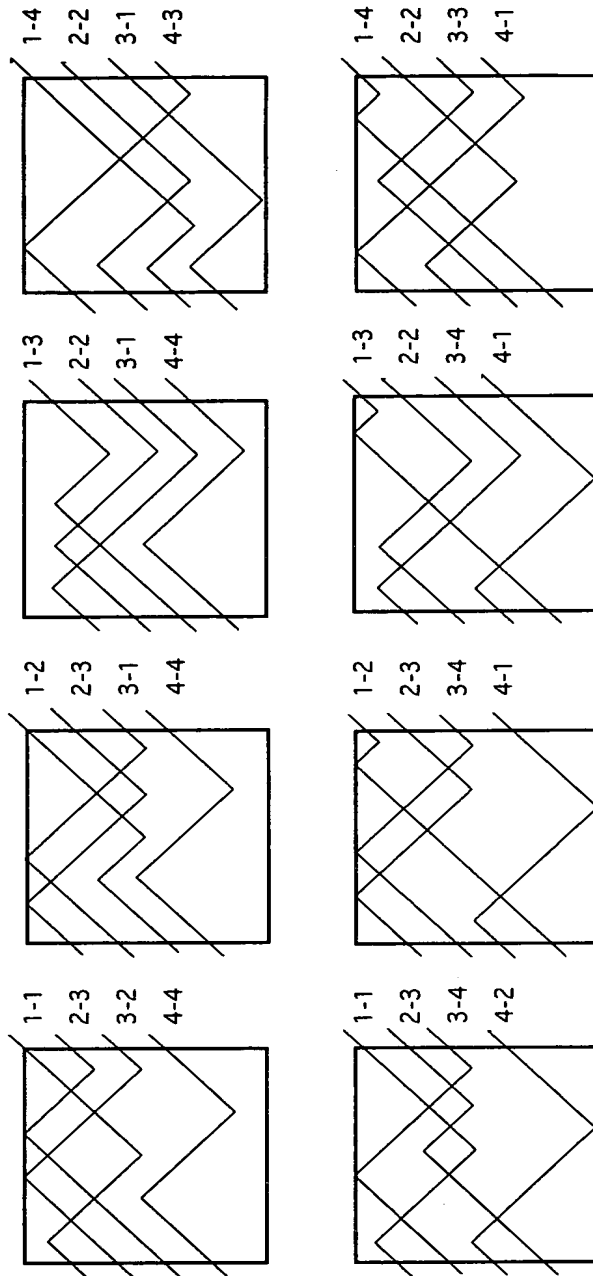


FIG. 40

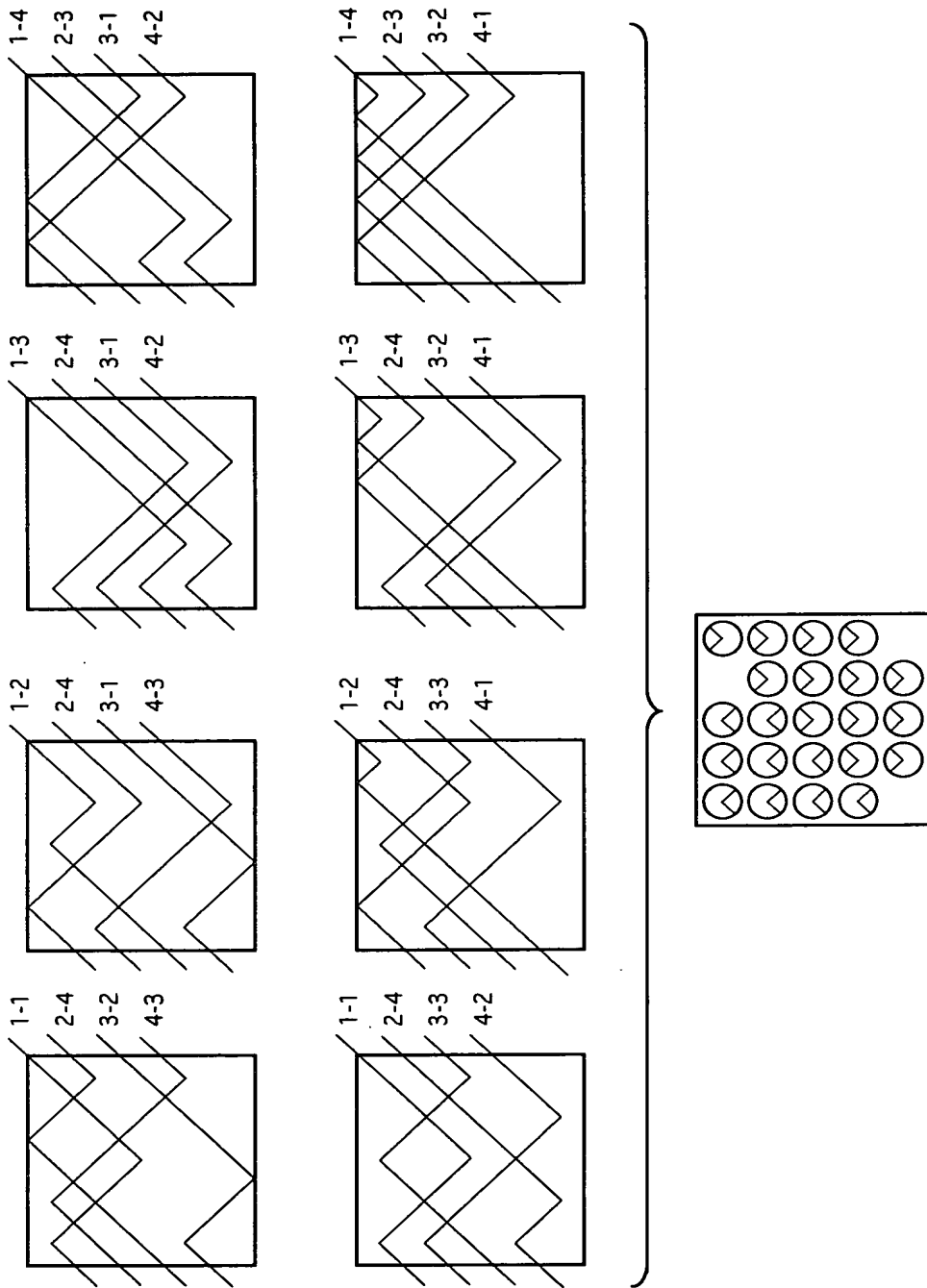


FIG.41

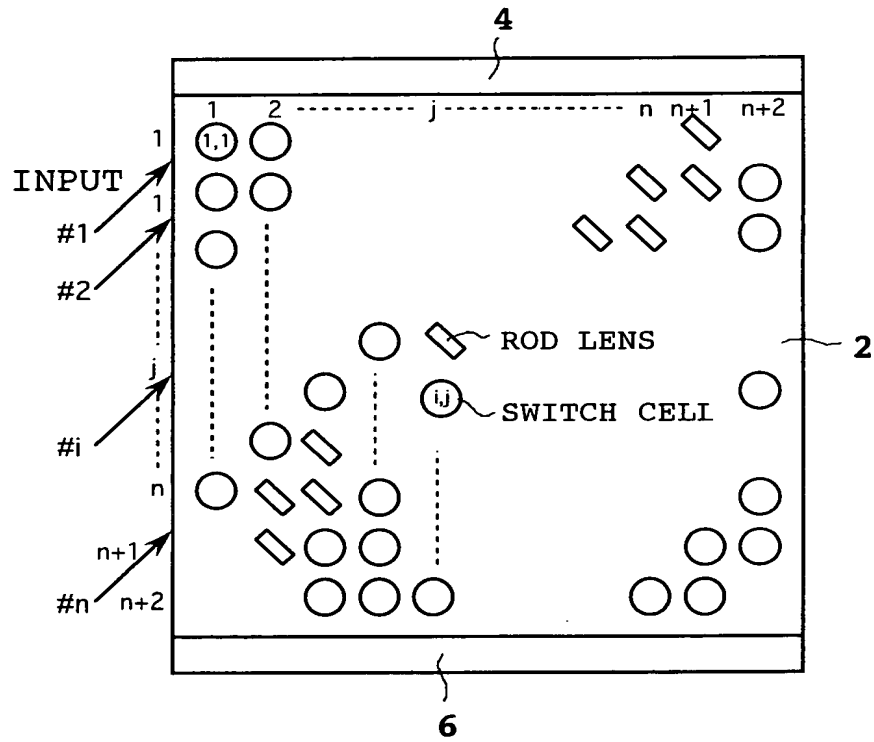


FIG.42

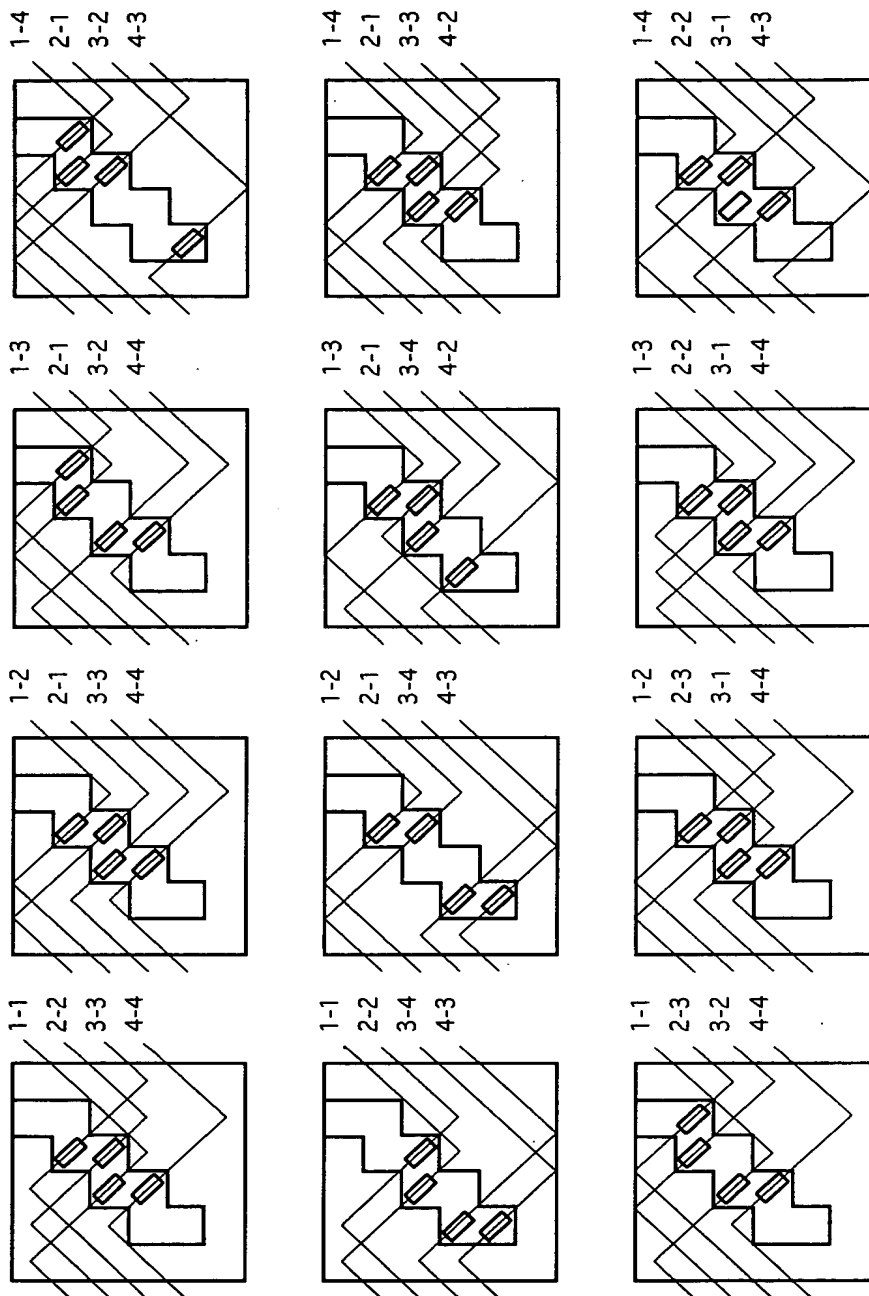


FIG.43

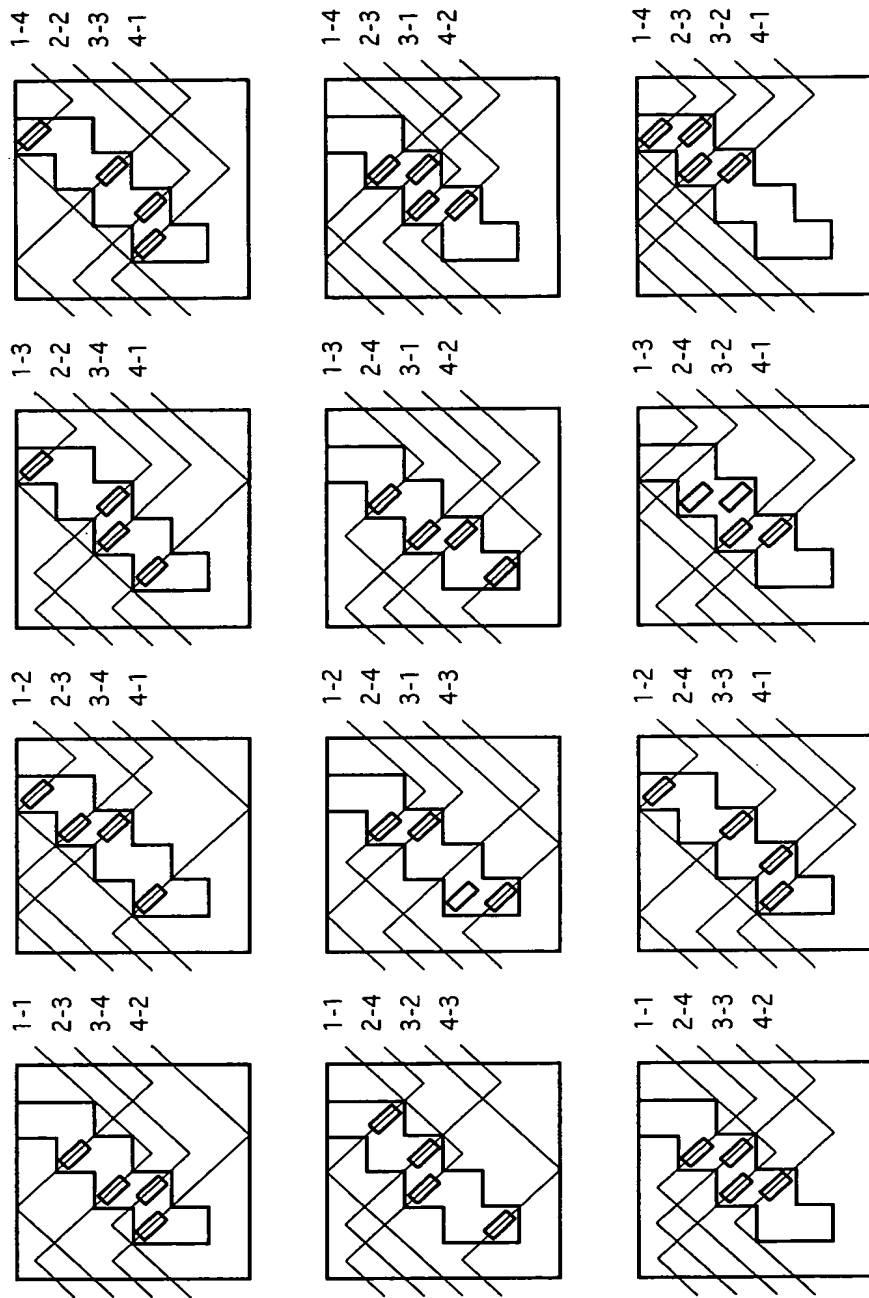


FIG.44

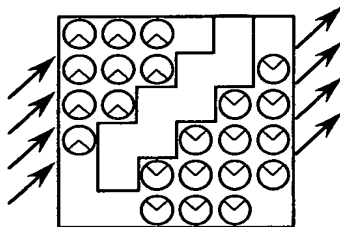
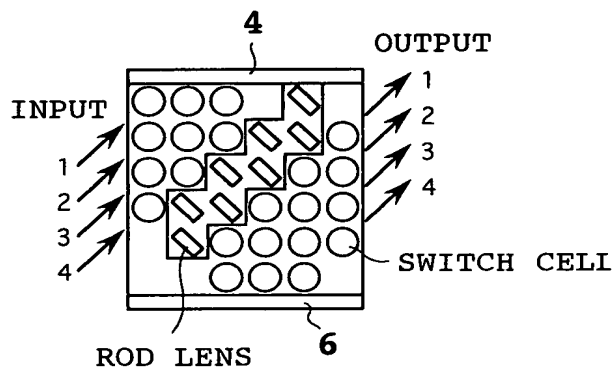
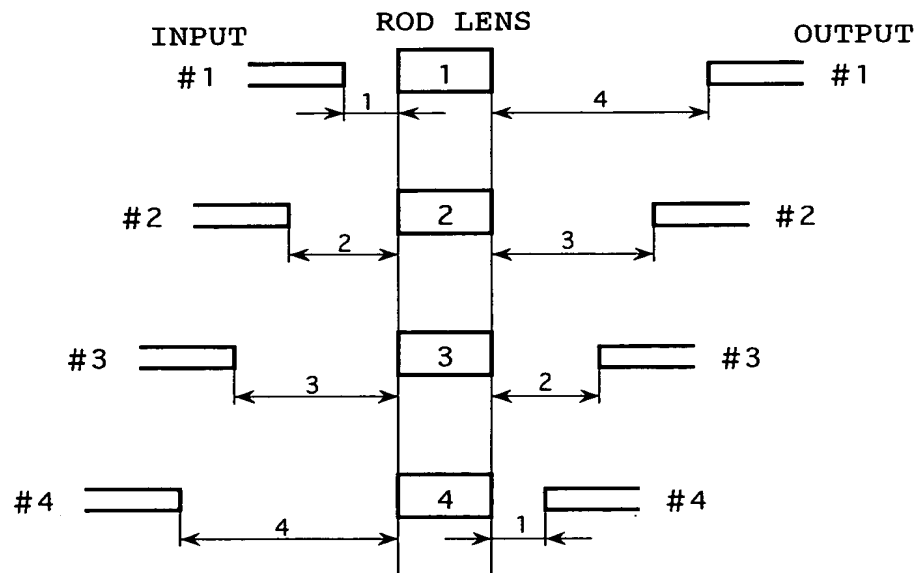
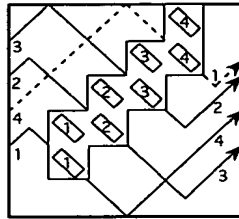


FIG.45



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FIG.46

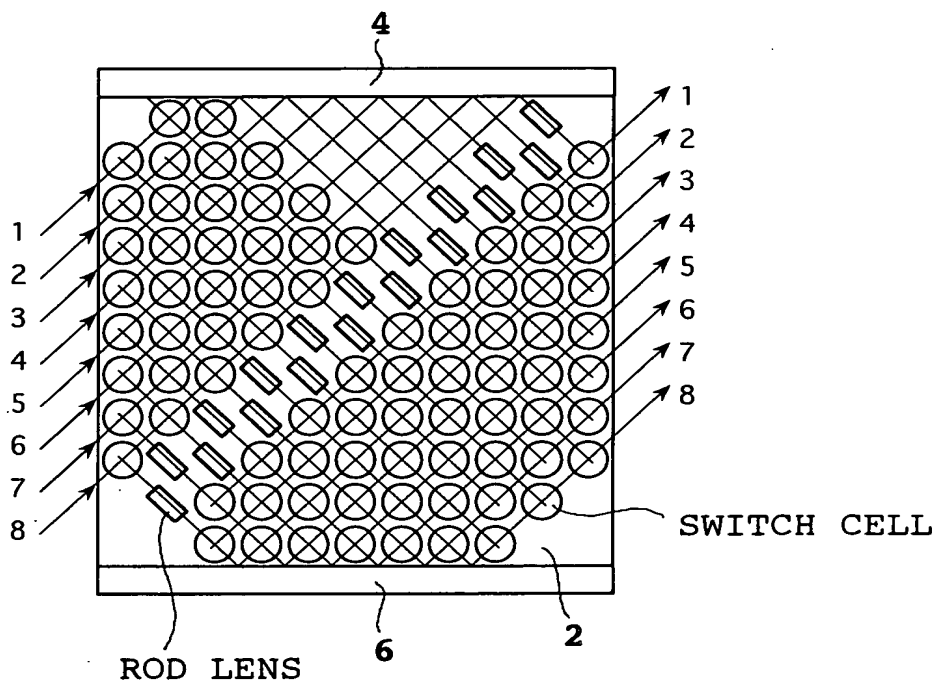


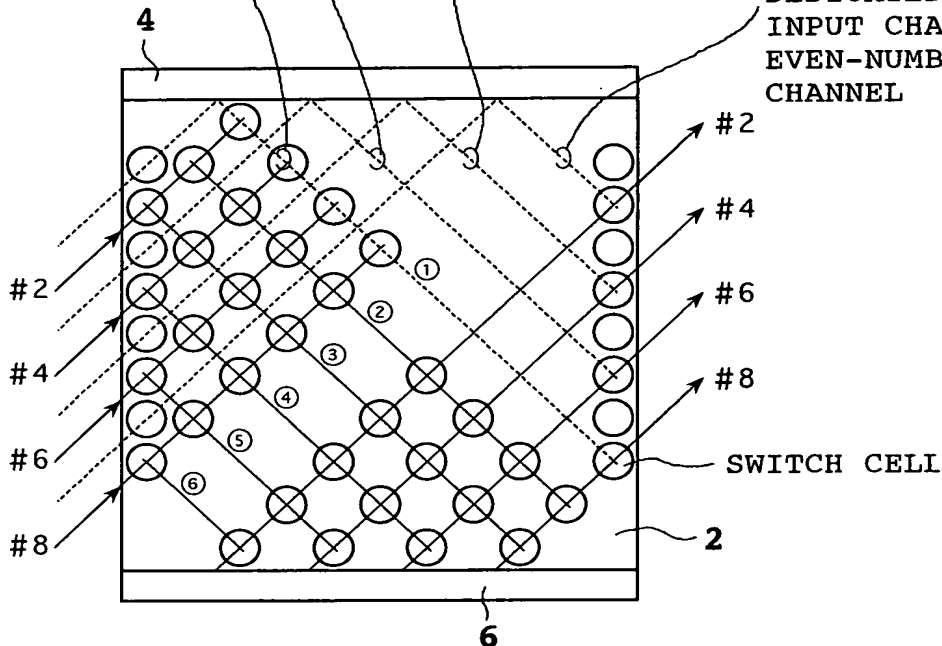
FIG.47

DEDICATED ROUTE FROM INPUT
CHANNEL #1 TO EVEN-NUMBERED OUTPUT CHANNEL

DEDICATED ROUTE FROM INPUT
CHANNEL #3 TO EVEN-NUMBERED OUTPUT CHANNEL

DEDICATED ROUTE FROM INPUT
CHANNEL #5 TO EVEN-NUMBERED OUTPUT CHANNEL

DEDICATED ROUTE FROM
INPUT CHANNEL #7 TO
EVEN-NUMBERED OUTPUT
CHANNEL



①, ②, ③ : ROUTES TO OUTPUT CHANNELS
#2, #4, #6, AND #8

④ : ROUTES TO OUTPUT CHANNELS
#2, #4, AND #6

⑤ : ROUTES TO OUTPUT CHANNELS
#2, AND #4

⑥ : ROUTES TO OUTPUT CHANNELS
#2

INPUT CHANNEL	ROUTE TO EVEN-NUMBERED OUTPUT CHANNEL
2	①/②/③
4	①/②/③, ④
6	①/②/③, ④, ⑤
8	①/②/③, ④, ⑤, ⑥

INPUT CHANNEL	OUTPUT CHANNEL	ROUTE
2 →	2	① or ② or ③
4 →	4	① or ② or ③
6 →	6	④
8 →	8	① or ② or ③

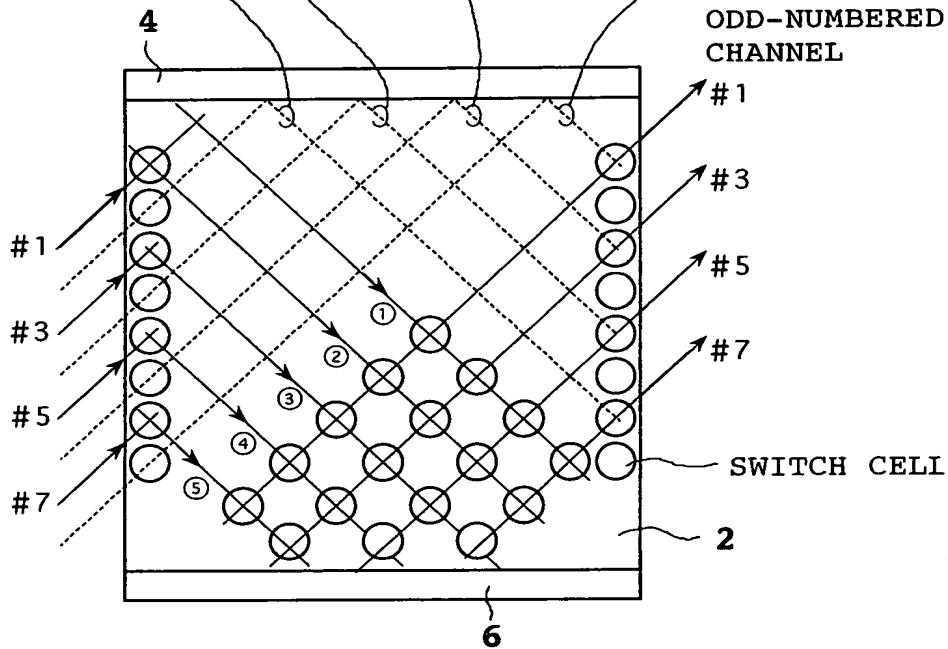
FIG.48

DEDICATED ROUTE FROM INPUT CHANNEL
#2 TO ODD-NUMBERED OUTPUT CHANNEL

DEDICATED ROUTE FROM INPUT CHANNEL
#4 TO ODD-NUMBERED OUTPUT CHANNEL

DEDICATED ROUTE FROM INPUT CHANNEL
#6 TO ODD-NUMBERED OUTPUT CHANNEL

DEDICATED ROUTE FROM
INPUT CHANNEL #8 TO
ODD-NUMBERED OUTPUT
CHANNEL



①, ② : ROUTES TO OUTPUT CHANNELS
#1, #3, #5, AND #7

③ : ROUTES TO OUTPUT CHANNELS
#1, #3, #5 AND #7 WHEN
INPUT CHANNEL IS #3, #5, OR
#7

④ : ROUTES TO OUTPUT CHANNELS
#1, #3, AND #5

⑤ : ROUTES TO OUTPUT CHANNELS
#1 AND #3

INPUT CHANNEL	ROUTE TO ODD-NUMBERED OUTPUT CHANNEL
1	①/②
3	①/②, ③
5	①/②, ③, ④
7	①/②, ③, ④, ⑤

INPUT CHANNEL	OUTPUT CHANNEL	ROUTE
1 →	1	① or ②
3 →	3	③
5 →	5	④
7 →	7	① or ②

FIG.49

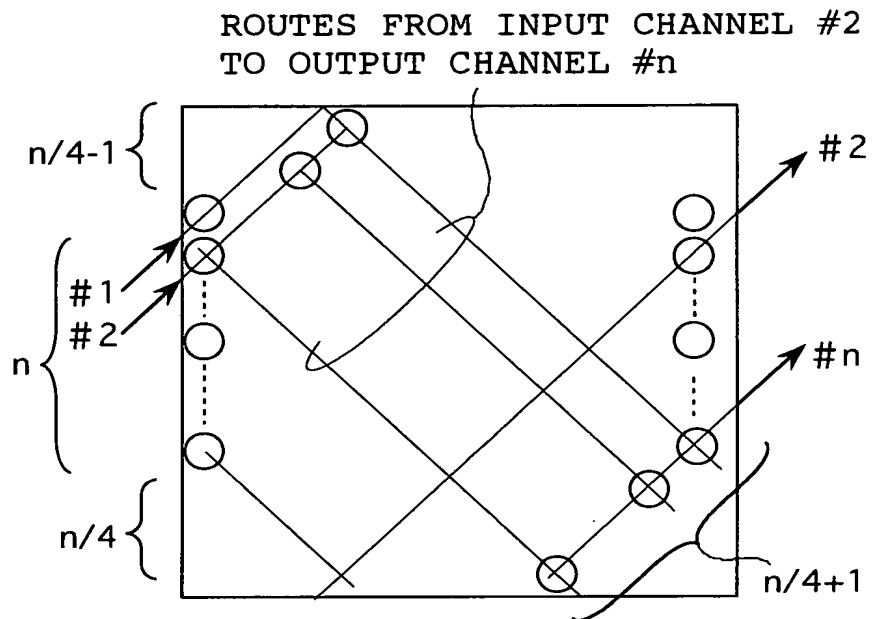


FIG.51

